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Wideband CMOS Low Noise Amplifiers

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ABSTRACT

Modern fully integrated receiver architectures, require inductorless circuits to achieve their potential low area, low cost, and low power. The low noise amplifier (LNA), which is a key block in such receivers, is investigated in this thesis.

LNAs can be either narrowband or wideband. Narrowband LNAs use inductors and have very low noise figure, but they occupy a large area and require a technology with RF options to obtain inductors with high Q. Recently, wideband LNAs with noise and distortion cancelling, with passive loads have been proposed, which can have low NF, but have high power consumption. In this thesis the main goal is to obtain a very low area, low power, and low-cost wideband LNA.

First, it is investigated a balun LNA with noise and distortion cancelling with active loads to boost the gain and reduce the noise figure (NF). The circuit is based on a conventional balun LNA with noise and distortion cancellation, using the combination of a common-gate (CG) stage and common-source (CS) stage. Simulation and measurements results, with a 130 nm CMOS technology, show that the gain is enhanced by about 3 dB and the NF is reduced by at least 0.5 dB, with a negligible impact on the circuit linearity (IIP3 is about 0 dBm). The total power dissipation is only 4.8 mW, and the active area is less than 50 x 50 μm^2 .

It is also investigated a balun LNA in which the gain is boosted by using a double feedback structure. We propose to replace the load resistors by active loads, which can be used to implement local feedback loops (in the CG and CS stages). This will boost the gain and reduce the noise figure (NF). Simulation results, with the same 130 nm CMOS technology as above, show that the gain is 24 dB and NF is less than 2.7 dB. The total power dissipation is only 5.4 mW (since no extra blocks are required), leading to a figure-of-merit (FoM) of 3.8 mW^{-1}, using 1.2 V

supply.

The two LNA approaches proposed in this thesis are validated by simulation and by measurement results, and are included in a receiver front-end for biomedical applications (ISM and WMTS), as an example; however, they have a wider range of applications.

Key-words: RC LNA, CMOS Wideband LNA, Noise and Distortion Cancelling, Active loads, RF Front–end Receivers.

RESUMO

As arquitecturas modernas de receptores completamente desenvolvidos em circuitos integrados, necessitam de circuitos sem bobinas para que as suas potencialidades de baixo custo, área reduzida e baixo consumo de energia possam ser atingidos. O amplificador de baixo ruído (LNA), que é um circuito essencial nestes receptores, é investigado nesta tese.

O LNA pode ser classificado quanto à sua largura de banda, nomeadamente, de banda estreita ou de banda larga. Os LNAs de banda estreita usam bobinas e têm geralmente um factor de ruído (NF) muito baixo, mas ocupam uma grande área e é imperativo que o seu fabrico seja realizado com uma tecnologia com opções de RF para obter bobinas com alto factor de qualidade (Q) o que encarece ainda mais o processo. Recentemente, têm sido propostos circuitos para LNAs de banda larga, com cancelamento de ruído e distorção, utilizando cargas passivas (i.e., resistências), que conseguem atingir um factor de ruído baixo, no entanto à custa de potências mais elevadas.

O objectivo principal desta tese é o projecto e desenvolvimento de um LNA de banda larga, com baixo consumo de energia, de área muito reduzida e consequentemente com um baixo custo de produção.

Numa primeira fase é investigado um LNA, com cancelamento de ruído e distorção, com recurso a cargas activas para aumentar o ganho e reduzir o factor de ruído. O circuito é baseado num LNA com cancelamento de ruído e distorção, que utiliza uma arquitectura já bem conhecida na literatura e que utiliza a combinação de um andar de porta comum (CG) e um outro de fonte comum (CS).

Os resultados de simulação e medições efectuadas aos circuitos projectados em tecnologia CMOS de 130 nm , mostram que o ganho é aumentado em cerca de

3 dB e o NF é reduzido em, pelo menos, 0,5 dB, com um impacto reduzido sobre a linearidade do circuito (IIP3 é cerca de 0 dBm), quando comparado com o mesmo circuito utilizando cargas passivas. A potência total dissipada é de apenas 4,8 mW, e a área efectiva é inferior a 50 x 50 mm^2.

Numa segunda fase, é investigado um LNA em que o ganho é ainda mais elevado, através da utilização de uma estrutura de realimentação dupla. A substituição de resistências por cargas activas, permite a implementação de realimentação local, através da injecção de sinal na porta dos transístores usados como carga activa. Isto permitirá aumentar ainda mais o ganho e reduzir o factor de ruído (NF).

Os resultados de simulação, para a mesma tecnologia CMOS de 130 nm previamente mencionada, mostram que o ganho é de 24 dB e NF é inferior 2,7 dB na banda de frequências de operação. A dissipação de potência total é de apenas 5,4 mW (sem recurso a circuitos auxiliares externos de polarização), o que se traduz numa figura de mérito de 3,8 mW^{-1}, para uma tensão de alimentação de 1,2 V.

As duas abordagens propostas nesta tese para a realização dos LNAs são validadas por simulação e medição dos protótipos implementados. Os circuitos propostos foram incluídos no projecto de um receptor sem-fios para banda larga com a finalidade de poder vir a ser utilizado em aplicações biomédicas (bandas ISM e WMTS), no entanto, pode ser utilizado em uma vasta gama de aplicações.

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ACRONYMS

f_t transition frequency.

BiCMOS Bipolar CMOS.

CG common-gate.

CMFB common-mode feedback.

CMOS complementary metal oxide semiconductor.

CS common-source.

DFB double feedback.

DFF double feedforward.

DT discrete-time.

DTMOS Dynamic Threshold MOS.

FFB feedforward and feedback.

FoM figure of merit.

GaAs gallium arsenide.

HBT heterojunction bipolar transistor.

IC integrated circuit.

IF intermediate frequency.

ISM industrial, scientific and medical.

LNA low noise amplifier.

MPW multi-project wafer.

NF noise figure.

RF radio frequency.

SDR software-defined radio.

Si silicon.

SiGe silicon-germanium.

SMA sub-miniature version A.

VCO voltage controlled oscillator.

WMTS wireless medical telemetry service.

WSN wireless sensor network.

CHAPTER 1

INTRODUCTION

1.1 Background and Motivation

In the last decades CMOS technology has been continuously subjected to down-scaling, mainly driven by digital applications in order to increase circuit speed and density. However, CMOS transistors have been considered slow devices for RF applications when compared to devices based on III-V compounds, since the electron saturated velocity is lower in Si [1].

Until recently, high and low frequency integrated circuits (ICs) were treated separately. The high frequency ICs could only be realized with large areas in more expensive technologies than standard CMOS, such as GaAs, SiGe, HBT, Bipolar, and BiCMOS [2]. This reduction of transistors' channel length lead to an increase of the transition frequency (f_t), defined as the short-circuit unity current gain frequency, up to hundreds of gigahertz and a reduction of power consumption, which made a challenge to implement analog radio frequency (RF) functions in CMOS technology. Furthermore, research efforts have been made to provide more accurate and compact device models for analog RF CMOS transistors.

The current proliferation of mobile communication systems and wireless sensor networks (WSNs) has increased the use of wireless devices in applications for

license free industrial, scientific and medical (ISM) and wireless medical telemetry service (WMTS) bands [3]. Therefore, there is a large demand for devices that have reduced cost and power consumption, while maintaining a reliable and efficient performance. The ultimate goal is to integrate the digital and analog RF circuits in one chip, which is now possible due to the advance of modern CMOS technologies. Modern fully integrated receiver architectures (e.g. Low-IF and Zero-IF), require inductorless circuits to achieve their potential low area, low cost, and low power [4]. The LNA, which is a key block in such receivers, is investigated in this thesis.

Narrowband LNAs use inductors and have very low noise figure, but they occupy a large area and require a technology with RF options to obtain inductors with high Q [5]. Wideband LNAs with multiple narrowband inputs have low noise, but their design is complex and the area and cost are high [6]. RC LNAs are very simple and inherently wideband, but their conventional realizations have large noise figure (NF). Recently, wideband LNAs with noise and distortion cancelling, with passive loads have been proposed, which can have low NF, but have high power consumption [7].

The mains focus of this PhD work is to investigate low noise amplifiers (LNAs), which are key blocks of wireless receivers, in particular low area, low power and low cost LNAs, which are required in ISM and WMTS bands for biomedical applications. However, a wideband LNA can be used in modern software-defined radio (SDR) receivers. Simulation and experimental results are provided which confirm the theoretical analysis.

It is used the LNA architecture employed in [8], with noise and distortion cancelling, which combines a common-gate (CG) stage and a common-source (CS) stage. In [8] resistor loads are used in these two stages. In this thesis, the resistor loads are replaced by MOS transistors, biased in moderate inversion and operating near the transition between triode and saturation, which allows the increase of the LNA gain (for the same voltage drop) and minimizes the circuit NF, without increasing the circuit die area; the active loads allow a supply voltage reduction, which can lead to a very low power consumption. This adds a new degree of freedom that allows the use of feedback and feedforward techniques for

gain enhancement and noise reduction, with minimum impact in linearity.

Two circuit prototypes have been designed in a standard 130 nm CMOS technology to compare the conventional design with resistors [8], and the new implementation, with active loads. We demonstrate that the proposed design methodology leads to a gain boost of 3 dB and reduces the NF by 0.5 dB. We also present a very low area and low cost LNA, with using a double feedback (DFB) technique to boost the gain and reduce the noise figure. A circuit prototype in a 130 nm standard CMOS technology at 1.2 V has been designed and simulated to demonstrate the proposed technique.

Simulation results show a gain of 24 dB and NF below 2.7 dB, with power dissipation of only 5.4 mW, leading to a figure of merit (FoM) of 3.8 mW. Measurement results of the proposed DFB LNA which is included in a modern receiver are also presented, proving that the proposed approach leads to a high gain, low NF circuit, when compared with other state-of-the art approaches.

1.2 Thesis Organization

This thesis is organized in seven chapters, including this introduction.

In Chapter 2, an overview of fundamental concepts for wireless receivers and LNAs is given. The conventional RF front-end architectures, where the LNA is included, are presented and the most common LNA topologies are briefly described. The main performance parameters and definitions relevant for receivers and in particular for LNAs are also introduced, such as impedance matching, noise figure, intermodulation products and FoMs.

Chapter 3 gives a review of the state-of-the art LNAs. It is focused on wideband architectures, which exploit several techniques that offer additional freedom in LNA design to overcome the trade-off between input matching and NF that is usually critical in design.

In Chapter 4 an LNA with active loads is investigated. It is shown that this configuration allows the implementation of an LNA with continuously controllable voltage gain. The impact on linearity is analysed in depth, and its performance

is compared with a similar version with resistive loads under the same bias conditions.

In Chapter 5 two LNA design approaches are introduced, namely double feedforward (DFF) and DFB . Through the use of local feedback techniques the gain can be maximized and the overall noise figure is reduced. The DFF LNA is particularly interesting under low supply voltage, and simulation results show that it is feasible and can achieve high gain with a supply of 0.6 V. The DFB LNA offers the best performance among the presented LNA topologies.

In Chapter 6, measurement results are presented. First, the LNAs implemented with resistors and with active loads are compared. Then the implementation of a modern RF front-end for low-IF receivers is discussed, where the proposed LNA is included. For comparison purposes, two versions of the RF front-end were designed and implemented, one using the LNA with active loads and the other using the proposed DFB LNA.

Finally, Chapter 7 is devoted to a discussion of the results. Conclusions are drawn and future work is suggested.

1.3 Original Contributions

The main contributions of this thesis are as follows.

We present a detailed balun LNA with active loads. This circuit is compared with the traditional design with resistive loads [9]. The active loads allow a continuously controllable gain. A complete theoretical analysis of linearity and noise has been done regarding the minimization of intermodulation products. The result this work has been published in [10].

In order to find alternative solutions to achieve higher gain and lower noise figure for the balun LNA with the new degree of freedom allowed by active loads, new topologies were investigated exploiting the use of local feedback without degradation of linearity. Based on this new approach, the following new circuit designs are proposed:

- A DFF LNA with high gain and under 0.6 V supply operation, with very low

power consumption, which is particularly useful for biomedical applications [11].

- An LNA in which the gain is boosted and the noise figure is reduced by using a double feedback structure [9].

Finally, measurement results are presented for the proposed LNA with active loads (without feedback) and for a DFB LNA, both included in a receiver front-end for biomedical applications (ISM and WMTS). These measurements prove that the proposed approach using double feedback leads to a high gain, low NF circuit, when compared with other state-of-the art approaches. This work has lead to a publication in a special issue of an international journal for RF design techniques [12].

CHAPTER 2

WIRELESS RECEIVERS AND LNAS

In this chapter, an overview of receiver architectures and of the conventional low noise amplifiers is made. The basic concepts and definitions used in wireless systems and main RF performance parameters used in LNAs and RF circuits are described to provide the background on which this PhD work is based.

2.1 Receiver Architectures

A communication system is composed of a transmitter, a receiver, and a communication channel, in which, the signal is propagated. On the transmitter side, the signal containing the information is included in a periodic signal, denominated carrier, through a process called modulation which consists of the variation of, at least, one of its characteristics, amplitude, frequency, or phase. The main function of the receiver is to recover the information contained in the original signal through a demodulation process.

In a wireless system, the signals are converted to high frequency for transmission and propagated through the air, and then down-converted to the baseband for reception. This conversion is necessary for two main reasons: the signals can carry more information at high frequencies (higher bandwidth) and small size antennas are required (the antenna size is typically proportional to the wavelength

of the signal). Although the communication medium is far from ideal, and the signal received is usually very weak (of the order of microvolts), and is also susceptible to interferences from other signals (that can be stronger). Therefore, it is necessary to eliminate unwanted signals and detect the information contained in the signal of interest. In the following sections, the main receiver architectures that are commonly used today are briefly described [4], [13].

2.1.1 Heterodyne Receiver

The heterodyne receiver topology, represented in Fig. 2.1, was proposed by Armstrong in 1918 [14] and is one of the most used architectures in wireless communication systems. The RF signal received by the antenna is filtered by a bandpass filter, thus minimizing the influence of near interferers, then it is amplified by a low noise amplifier and down-converted to a lower, intermediate frequency (IF), through a signal multiplier (mixer), to which the output of a local oscillator (LO) is applied. At the mixer output there is a bandpass filter at the IF, called the channel selection filter, which isolates the desired signal from signals in adjacent channels. The signal demodulation is usually done in the digital domain and, therefore, it is necessary to include an analog to digital converter (ADC), followed by a digital signal processor to perform the demodulation process.

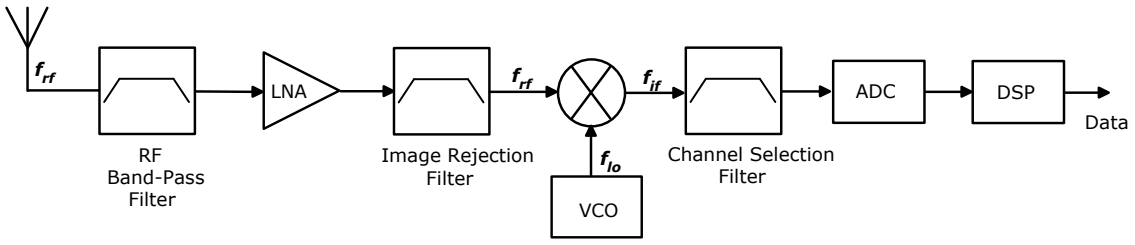


Figure 2.1: Heterodyne Receiver.

The main advantage of this architecture is that the IF is fixed, so the desired frequency is selected by tunning the LO, making it easier to design the channel selection filter, which should be very selective, with a high quality factor (Q). However, a major problem can occur if at the mixer input also exists a signal, called image signal, with frequency $f_{im} = 2f_{lo} - f_{rf}$, as shown in Fig. 2.2. This signal

after the multiplication originates at the mixer output two signals at frequencies $f_1 = f_{lo} - f_{rf}$ and $f_2 = 3f_{lo} - f_{rf}$, and since f_1 coincides with the intermediate frequency, it overlaps the signal of interest, and it is impossible to separate the two signals.

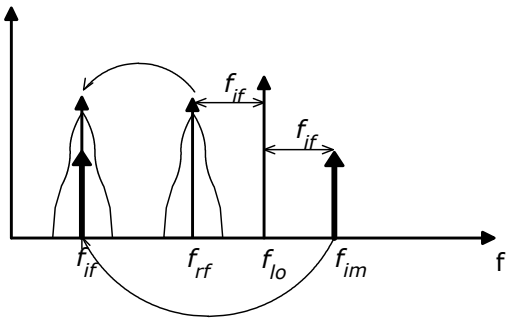


Figure 2.2: Frequency spectrum showing the image signal.

A filter is necessary before the mixer to reject the image signal (image rejection filter). Furthermore, the frequency difference between RF and image signals is $2f_{if}$, hence, increasing f_{if} relaxes the image rejection filter specifications. However, as f_{if} increases, the channel selection filter must have tighter specifications for the same bandwidth, because the quality factor Q, which is proportional to the centre frequency, increases. Filters with a high Q are difficult to realize with CMOS technology, and so there is a trade-off between intermediate frequency and quality factor. In practice, high performance filters must be realized externally, which makes on chip full integration impractical.

2.1.2 Homodyne or Zero-IF Receiver

To overcome the difficulty of implementing a fully integrated heterodyne receiver, another receiver architecture is employed, commonly referred to as homodyne, direct conversion, or "Zero-IF". In the direct conversion receiver, the RF signal is converted directly to the baseband by using an LO with the same frequency as the RF signal, which eliminates the problem of the image rejection; thus, the image rejection filter is no longer required. Moreover, with the signal of interest in the baseband, the channel selection filter can be replaced by a low-pass filter which is easier to design and implement.

In Fig. 2.3(a) a simplified direct conversion receiver is represented which is suitable for double-sideband amplitude modulation (AM) signals, since, after the down conversion, both sidebands are overlapped in the baseband, carrying the same information. However, for more sophisticated modulation schemes, such as frequency modulation (FM) or quadrature phase-shift keying (QPSK), the sidebands may carry different information, and in order to avoid loss of information after the down conversion, a quadrature architecture is used as shown in Fig 2.3(b).

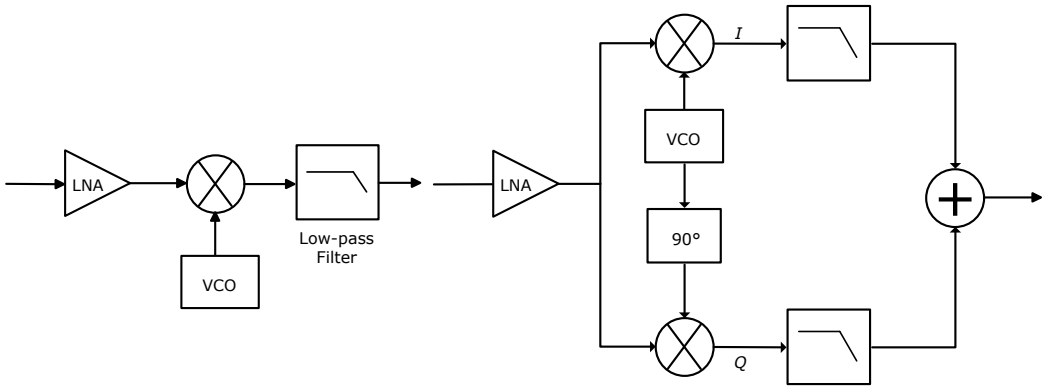


Figure 2.3: Homodyne receiver: (a) single receiver (b) quadrature receiver.

Despite its low complexity, this architecture presents some drawbacks, described below, that prevent it from being applied in some cases.

DC offsets One problem is related to leakages between the LO port and the LNA and mixer inputs, when the ports are inadequately isolated, due to substrate and capacitive coupling. When a leakage signal from the LO appears at the inputs of LNA and mixer, there is a "self-mixing" effect that originates a DC component at the mixer output, which can lead to saturation of the following stages. A similar effect occurs if there is a leakage from the LNA or mixer input to the LO port of the mixer.

I/Q Mismatch As referred above, with frequency or phase modulation, quadrature signals are required and ideally they should have the same amplitude and

a phase difference of 90°. However, the circuits are not ideal and imbalances between I and Q signals are expressed as gain and phase errors. The result of this "I/Q mismatch" is a corruption of the received signal constellation, which would cause a degradation of the system performance such as an increase of the bit error rate (BER).

Even order distortion If the LNA has a second order nonlinearity such as $y(t) = a\ x(t) + b\ x^2(t)$, and if near the channel of interest there exist two close interferers, $x(t) = A_1\ cos(\omega_1 t) + A_2\ cos(\omega_2 t)$, one of the resulting output terms is $b\ A_1\ A_2\ cos((\omega_1 - \omega_2)t)$. This indicates that one of the interferers component is near the baseband ($\omega_1 - \omega_2$), and in the case of an ideal mixer, there is no problem, because, after multiplication by the LO signal, this component is shifted to high-frequencies. However, the mixers are not ideal and exhibit some feed-through directly to the output, so part of the interferer appears at the output at the baseband, together with the down converted signal, which leads to signal distortion.

To avoid this problem, differential LNAs and mixers should be employed in order to eliminate even order harmonics, but this implies more power consumption and larger circuit area.

Flicker noise Another drawback is the existence of “flicker noise” that is more significant for low frequencies, specially for MOSFETS. This noise causes signal degradation if it appears in the baseband, at the mixer output. The flicker noise subject is further discussed in section 2.2.

In spite of their simplicity, homodyne receivers are impractical for some applications, although there are techniques to solve some of the above mentioned drawbacks by adding additional complexity to the circuit.

2.1.3 Low-IF Receiver

The low-IF topology combines the advantages of both types of receivers, heterodyne and homodyne, by using a mixed approach, i.e, by using a low intermediate frequency. This relaxes the channel selection filter specifications and simultaneously avoids the problems related to direct conversion, in particular the flicker noise that strongly affects the baseband signal. To overcome the image problem associated with the heterodyne receiver, a technique to cancel the image signal is employed in order to avoid the image rejection filter. The image cancellation is achieved by using quadrature architectures, in which the image is suppressed after generating a negative replica.

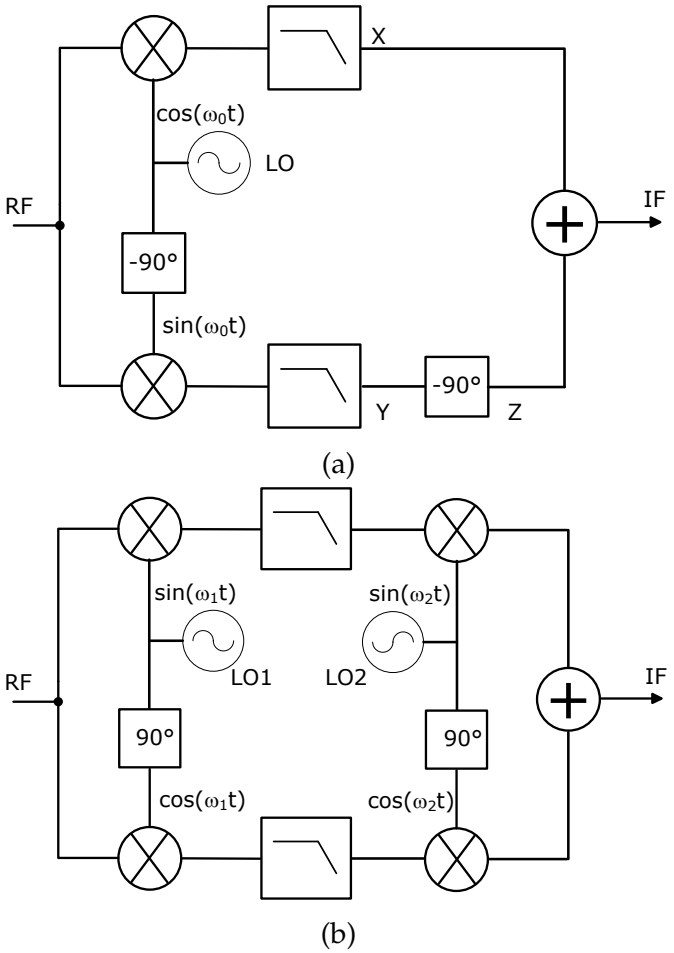


Figure 2.4: Image rejection architectures: (a)Hartley (b)Weaver.

The Hartley [15] architecture shown in Fig. 2.4(a), is one of the alternatives to cancel the image signal. If at input there is the signal and the corresponding image

$x(t) = V_{RF}\ cos(\omega_{RF}t) + V_{Im}\ cos(\omega_{Im}t)$, after down conversion and filtering the resulting signals at X and Y are, respectively:

$$x(t) = \frac{V_{RF}}{2}cos((\omega_{RF} - \omega_{LO})t) + \frac{V_{Im}}{2}cos((\omega_{LO} - \omega_{Im})t) \tag{2.1}$$

$$y(t) = -\frac{V_{RF}}{2}sin((\omega_{RF} - \omega_{LO})t) + \frac{V_{Im}}{2}sin((\omega_{LO} - \omega_{Im})t) \tag{2.2}$$

Since $sin(\theta - \frac{\pi}{2}) = -cos(\theta)$, after a -90° shift, the signal at Z is,

$$z(t) = \frac{V_{RF}}{2}cos((\omega_{RF} - \omega_{LO})t) - \frac{V_{Im}}{2}cos((\omega_{LO} - \omega_{Im})t) \tag{2.3}$$

Finally, by adding the signals at X and Z, the wanted signal is recovered and the image is suppressed. The Weaver [16] architecture (Fig. 2.4(b)) produces a similar result, and the second LO frequency can be chosen to achieve a direct conversion to the baseband. However, both circuits are susceptible to "I/Q mismatch", as referred above, leading to incomplete image rejection.

The low-IF topology allows a flexible compromise between the Zero-IF and Heterodyne topologies.

2.1.4 Wideband Receiver

The wideband receiver is becoming more popular among the receiver architectures, due to its flexibility to accommodate multi-band and multi-standard wireless communications, inspired by software defined radio [17]–[19]. Differently from conventional RF front-ends, the wideband receiver does not have a filtering stage after the antenna: therefore, it is fully exposed to the spectrum, which is crowded of out-of-band interferers and signals from the several wireless standards that are ubiquitous these days, and consequently, in the absence of filtering, these interferers have direct impact on the dynamic range and sensitivity of the system.

A strong effort has been made in the development of low cost and low area wideband receivers, which can be software defined for different bands and specifications [20]. This type of receivers typically down converts the RF signal to a low intermediate frequency or directly to the baseband (direct conversion). However, this flexibility presents some design challenges in the analog front-end. In Fig. 2.5,

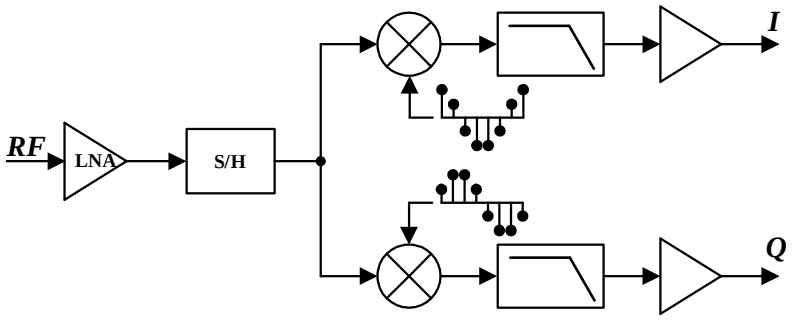


Figure 2.5: Wideband SDR RF front-end receiver [18].

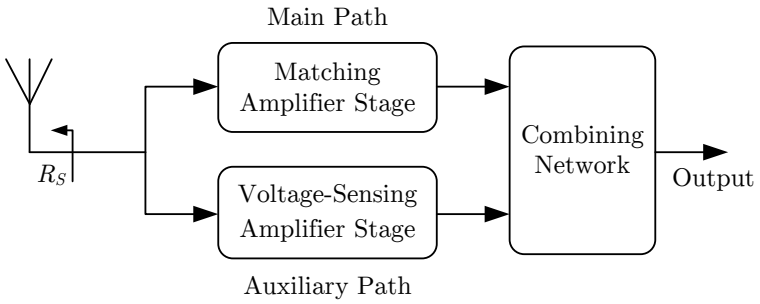


Figure 2.6: Noise and distortion cancelling principle [21].

a general architecture of a wideband RF front-end receiver is shown. In the example, a discrete-time (DT) passive mixer is used, driven by a multi-phase square wave oscillator. Passive mixers with hard switching are usually preferred due to their good linearity, and by combining the sum of properly weighted poly-phase clock signals, wideband harmonic rejection can be achieved, therefore, relaxing the filters specifications [18], [21]·

In order to obtain a receiver with low noise and low distortion, a noise and distortion cancelling principle can be used, which can be done at circuit level (e.g., LNA) or in the overall receiver, as shown in Fig. 2.6. Basically the input signal is divided into two branches: the main signal path and an auxiliary path for sensing, which are then combined at the output of the LNA or at the Low IF after the downconversion in the case of a receiver[20].

In this type of receivers the LNA is a critical block, which will set the performance of the complete receiver. A wideband LNA is required that can provide a stable input matching on the entire band of interest, with enough gain not to compromise the overall linearity, while at the same time the NF must be very low.

Thus, the main motivation of this thesis is to design a CMOS wideband LNA, suitable to be used in wideband receivers for biomedical applications.

2.2 LNA Performance Parameters

2.2.1 Impedance Matching

Lumped circuit analysis assumes that the network's dimensions are much smaller than the electromagnetic wavelength, and therefore, the signal propagation over the network is practically instantaneous. However, for high frequencies the wavelength tends to be of the same order of the circuit dimensions, and consequently the circuit paths behave like transmission lines, which require distributed parameter analysis. When a transmission line is terminated by a load Z_L, the voltage reflection coefficient defines the amplitude of a reflected voltage wave (V_o^-) normalized to the incident wave amplitude (V_o^+), as follows [22]:

$$\Gamma = \frac{V_o^-}{V_o^+} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.4}$$

where Z_0 is the transmission line characteristic impedance. To achieve the maximum power transfer to the load, there should be no reflection, i.e, $\Gamma = 0$, which only occurs when $Z_L = Z_0$, and then the load is matched to the line characteristic impedance. Usually in RF systems the antenna has a characteristic impedance of 50 Ω, so the first block of a receiver must have the input impedance of 50 Ω.

2.2.2 Scattering Parameters

At high-frequencies, the usual system characterization used in low frequencies trough open and short-circuit measurements is more difficult than measuring the average power, because currents and voltages measurements involve the magnitude and phase of the travelling waves [23]. For that reason, at high-frequencies (when the device length is not negligible with respect to the wavelength) different parameters are required for network characterization. The scattering parameters

(S-parameters) relate the power of incident and reflected waves, at n-ports, trough the scattering matrix,

$$\begin{bmatrix} b_1 \\ \vdots \\ b_n \end{bmatrix} = \begin{bmatrix} S_{11} & \cdots & S_{1n} \\ \vdots & & \vdots \\ S_{n1} & \cdots & S_{nn} \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ \vdots \\ a_n \end{bmatrix} \tag{2.5}$$

where, a_n is the incident power wave at port n and b_n corresponds to the reflected wave. A specific s-parameter is determined as follows,

$$S_{ij} = \left. \frac{b_i}{a_j} \right|_{a_k=0,\ k \neq j} \tag{2.6}$$

which physically means that an s-parameter gives the ratio between the reflected wave at port i and the incident wave at port j when the other ports are terminated with a matched load to avoid unwanted reflections. The s-parameters are measured directly with a network analyser, and allow an accurate network characterization without knowing in detail the circuit inside the network.

For the particular case of a two-port network (Fig.2.7) the s-parameters are designated according to their physical meaning [22]:

- S_{11} - Input reflection coefficient
- S_{21} - Forward power gain
- S_{12} - Reverse power gain
- S_{22} - Output reflection coefficient

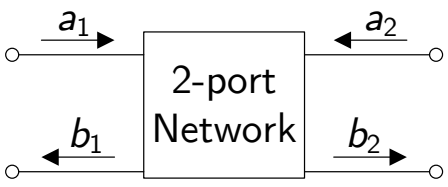


Figure 2.7: Two-Port Network with the incident and reflected waves.

In receiver front-ends, the s-parameters are particularly useful in LNA design due the need of input matching, and are associated with the concept of return loss. The return loss is a figure of merit for signal reflection and indicates the fraction of the incident power that is reflected back to the source. LNAs technical specifications usually include the input return loss, defined as [24],

$$\mathrm{RL} = -20\log(|S_{11}|) \tag{2.7}$$

It is desirable to minimize the reflected power, so more power is transferred to the load. Typically, designers aim for at least 10 dB return loss, as the requirements for wireless systems often specify a 10 dB return loss bandwidth [25].

2.2.3 Noise

Noise arises in electronic circuits as a random variable, caused by physical phenomena due to the nature of the materials or by external interferences. Noise is non deterministic and its instantaneous value can not be foreseen. The presence of noise in circuits is inevitable, and, therefore, it is important to analyze its impact on the degradation of signals of interest and develop methods to minimize its effect. In this section the main noise sources present in CMOS devices are described [6], [26].

2.2.3.1 Thermal Noise

Thermal noise in circuits is due to the random motion of electrons, causing a variation of current. The thermal noise power can be expressed as

$$P = kT\Delta f \tag{2.8}$$

where T is the temperature T (Kelvin), k is the Boltzmann's constant and Δf is the bandwidth of the system. In a resistor, the noise voltage generated is

$$\overline{V_{th}^2} = 4kTR\Delta f \tag{2.9}$$

and can be modeled by a voltage source in series with the resistor or by a current source in parallel with it, as shown in Fig. 2.8.

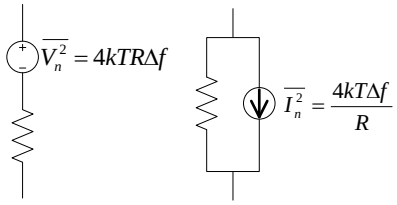


Figure 2.8: Resistor thermal noise models.

MOS transistors also exhibit thermal noise due to the carrier motion through the channel, and this noise can be represented by a current source in parallel with the conducting channel (Fig. 2.9). The noise generated when the device is operating in the triode region is [27]:

$$\overline{I_n^2} = 4kT\gamma g_{d0}\Delta f \tag{2.10}$$

where g_{d0} is the drain-source conductance for $V_{DS} = 0$ and γ is the excess noise factor and has a value of unity. However, the value of γ can change under different conditions. For long-channel MOSFET devices operating in saturation [28],

$$\overline{I_n^2} = 4kT\gamma g_m\Delta f \tag{2.11}$$

is generally assumed $\gamma = 2/3$ [29]. For short-channel and submicron MOSFETS, γ has higher values, in a range between 1 and 3 [30].

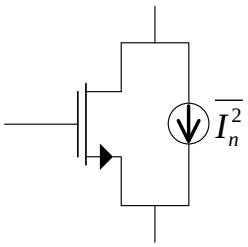


Figure 2.9: Mosfet thermal noise representation.

For further analysis and notation simplicity it is assumed that $\Delta f = 1$ Hz, expressing the noise per unit bandwidth.

2.2.3.2 Gate Noise

In addition to the intrinsic channel noise of the MOS transistor, there is another source of the thermal noise due to the distributed gate resistance, which can be critical as the channel length (L) decreases. This gate resistance is dependent on the MOS geometry and has two major contributions: the silicide sheet resistance (resistance of one square), and the contact resistance between the silicide and polysilicon. According to [31], the gate resistance for a single polysilicon gate finger, connected on both sides is:

$$R_G = \frac{1}{12}\rho_{sh}\frac{W}{L} + \frac{\rho_{con}}{WL} \tag{2.12}$$

where ρ_{sh} is the silicide sheet resistance, and ρ_{con} is the silicide-to-polysilicon contact resistance.

The equivalent noise model can be represented by a lumped resistor, with an equivalent gate resistance of $R_G/3$ in series with a voltage noise source ($\overline{V_{n,R_G}{}^2}$) with a power spectral density of $4kT\frac{R_G}{3}$, applied at the gate [32], [33], as shown in Fig. 2.10

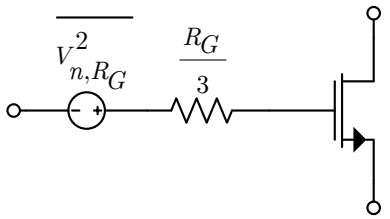


Figure 2.10: Equivalent noise model for gate resistance.

The influence of this noise source can be significantly reduced by proper design, since the effective silicide sheet resistance can be considerably reduced by the use of several gate fingers [31], [34]. Moreover, the impact of this noise on the circuit can be minimized if it is much lower than the channel noise, i.e., $4kT\frac{R_G}{3} << \frac{4kT\gamma}{g_m}$ [32].

2.2.3.3 Flicker Noise

The flicker noise in FETs has origin in a physical phenomenon, somewhat unpredictable, that is related with the interface between the gate oxide (SiO_2) and silicon

substrate (Si). The random fluctuation of the number of carriers in the channel is caused by trapping and release of carriers in the $Si - SiO_2$ interface. Flicker noise is proportional to $1/f$, so it is dominant at low frequencies. It is represented by a voltage source in series with the gate with spectral density

$$\overline{V_{nf}^2} = \frac{k_f}{C_{ox}\, W\, L\, f^{\alpha_f}} \tag{2.13}$$

where k_f is a process dependent constant, which is bias independent and, C_{ox}, W, and L, are the gate oxide capacitance per unit area, width, and length of the MOSFET, respectively. A cleaner fabrication process results in lower values for k_f. For p-channel devices k_f is lower than for n-channel devices, and, thus, PMOS transistors have less flicker noise. The exponent α_f is close to unity, and can have values between 0.7 and 1.2 [28]. This type of noise is still subject of study concerning its origins and modelling.

2.2.3.4 Shot Noise

Shot noise is caused by fluctuation of the current that crosses a potential barrier, such as in a pn-junction. The diffusion of charge carriers, which is random, causes the carriers to have different speeds, originating the fluctuation of current around an average value. The equivalent noise source is given by

$$\overline{I_{ns}^2} = 2qI_{DC} \tag{2.14}$$

where q is the electron charge and I_{DC} is the DC current. Shot noise is more significant in bipolar transistors, because both emmiter and collector currents are sources of shot noise, since they cross pn-junctions. In MOSFETs, the DC gate leakage current contributes with shot noise, but it is usually very small and in most cases it can be neglected.

2.2.3.5 Noise Figure

The noise factor, F, or noise figure, NF, when expressed in dB, is the most common measure of the noise generated by a circuit (characterized as a 2-port network).

The noise factor is defined as the ratio between the total noise power at the 2-port output and the 2-port output noise power due to the input noise source only:

$$F = \frac{Total\ output\ noise\ power}{Output\ noise\ due\ to\ the\ source} \tag{2.15}$$

Fig. 2.11 shows a noisy 2-port with power gain A. The noise factor is

$$F = \frac{N_2}{A^2 N_1} \tag{2.16}$$

where N_2 is the total noise power available at the output and N_1 is the noise power available at the 2-port input.

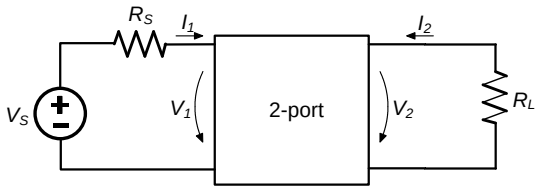


Figure 2.11: Noisy 2-port with gain A

If the ports are adapted and a power signal S_1 is applied from generator, then by the maximum power transfer theorem, the signal power is transferred entirely to the 2-port, and so is the signal power S_2 from the 2-port output to the load resistor R_L. The power gain is

$$A^2 = \frac{S_2}{S_1} \tag{2.17}$$

so,

$$F = \frac{N_2}{A^2 N_1} = \frac{\frac{S_1}{N_1}}{\frac{S_2}{N_2}} = \frac{(S/N)_i}{(S/N)_o} \tag{2.18}$$

The last equation relates the noise factor with the signal to noise ratios at the input and output of the 2-port, which shows the degradation of the signal to noise ratio due to the noise introduced by the 2-port. When no additional noise is introduced by the 2-port, $F = 1$.

2.2.4 Linearity

The performance related to linearity can be characterized by the 1 dB compression point and by the 2nd and 3rd-order intermodulation products. These parameters appear in the systems specification.

A linear system when excited by an input signal generates an output signal proportional to the input. Most devices have a non-linear characteristic, and if they are memoryless and time invariant, then their operation can be represented by a Taylor series, i.e,

$$y = a_0 + a_1 x + \ldots + a_n x^n \tag{2.19}$$

The terms used to represent these devices depends on the type of non-linearity, being its representation more accurate if more terms are used.

2.2.4.1 Harmonics and Intermodulation Products

Nonlinear devices generate harmonics. A nonlinear device characterized by a third-order polynomial is usually a good approximation, that simplifies the calculations. If the input signal is sinusoidal,

$$v_i(t) = V_m cos(\omega_f t) \tag{2.20}$$

the output is

$$y(t) = a_0 + a_1 V_m cos(\omega_f t) + a_2 V_m^2 cos^2(\omega_f t) + a_3 V_m^3 cos^3(\omega_f t) \tag{2.21}$$

or

$$y(t) = \underbrace{a_0 + \frac{a_2 V_m^2}{2}}_{DC\ component} + \underbrace{\left(a_1 V_m + \frac{3a_3 V_m^3}{4}\right) cos(\omega_f t)}_{1^{st} Harmonic (fundamental)} + \underbrace{\frac{a_2 V_m^2}{2} cos(2\omega_f t)}_{2^{nd} Harmonic} + \underbrace{\frac{a_3 V_m^3}{4} cos(3\omega_f t)}_{3^{rd} Harmonic} \tag{2.22}$$

A nonlinearity of order n generates n harmonics with multiples of the fundamental frequency ($n\,\omega_f$). The even order coefficients affect the DC component, whereas the odd order coefficients have impact on the fundamental frequency amplitude.

If, instead of applying a single sinusoidal signal at the non-linear device input, two signals are applied with different frequencies:

$$v_i(t) = V_1 cos(\omega_1 t) + V_2 cos(\omega_2 t) \tag{2.23}$$

intermodulation products are generated at the output, given by:

$$\begin{aligned} y(t) =& a_0 + a_1(V_1 cos(\omega_1 t) + V_2 cos(\omega_2 t)) + \\ & a_2 \left[\begin{array}{c} \frac{V_1^2}{2}(1 + cos(2\omega_1 t)) + \frac{V_2^2}{2}(1 + cos(2\omega_2 t)) + \\ V_1 V_2(cos((\omega_1 + \omega_2)t) + cos((\omega_1 - \omega_2)t)) \end{array} \right] + \\ & a_3 \left[\begin{array}{c} \left(\frac{3}{4}V_1^3 + \frac{3}{2}V_1 V_2^2\right) cos(\omega_1 t) + \left(\frac{3}{4}V_2^3 + \frac{3}{2}V_2 V_1^2\right) cos(\omega_2 t) + \\ \frac{3}{4}V_1^2 V_2(cos((2\omega_1 + \omega_2)t) + cos((2\omega_1 - \omega_2)t)) + \\ \frac{3}{4}V_2^2 V_1(cos((2\omega_2 + \omega_1)t) + cos((2\omega_2 - \omega_1)t)) + \\ \frac{3}{4}V_1^3 cos(3\omega_1 t) + \frac{3}{4}V_2^3 cos(3\omega_2 t) \end{array} \right] \end{aligned} \tag{2.24}$$

In addiction to harmonics, intermodulation products appear at frequencies $n\,\omega_1 \pm m\,\omega_2$. Fig. 2.12 illustrates the intermodulation products for a particular case of a nonlinearity of order 3.

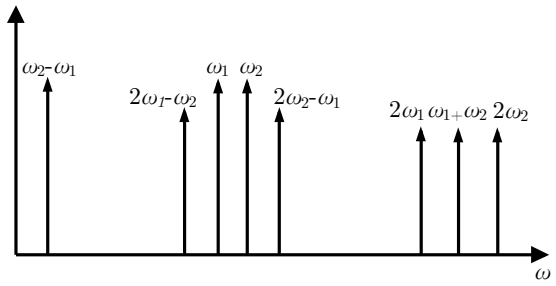


Figure 2.12: Frequency spectrum showing the intermodulation products of a nonlinear device of order 3.

2.2.4.2 1 dB Compression Point

The 1 dB compression point is a linearity measure of a circuit and is defined as the output signal power that corresponds to a difference of 1 dB from the ideal (linear) circuit, as shown in Fig. 2.13. At that point, the compression is reached which consequently degrades the signal.

2.2.4.3 Intercept Points

The n^{th} order intercept point (IPn) is defined as the point at which the curves of power output of the fundamental frequency and of the n^{th} intermodulation

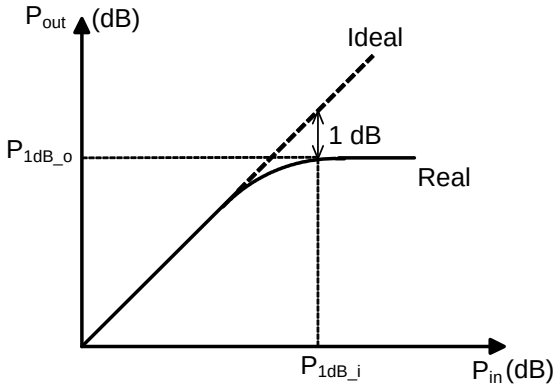


Figure 2.13: Definition of 1 dB compression point.

product would intercept if they were linear (asymptotically extrapolated), i.e, when the amplitude of the fundamental frequency would be equal to the amplitude of the n^{th} intermodulation product. The specifications for intercept points are often input-referred $IIPn$, but can also be output-referred $OIPn$, as illustrated in Fig. 2.14. The most commonly intercept points used to characterize a LNA are $IP2$ and $IP3$. A practical rule that is employed in most radio frequency amplifiers is that the 1 dB compression point falls at least 10 dB below the third order intercept point.

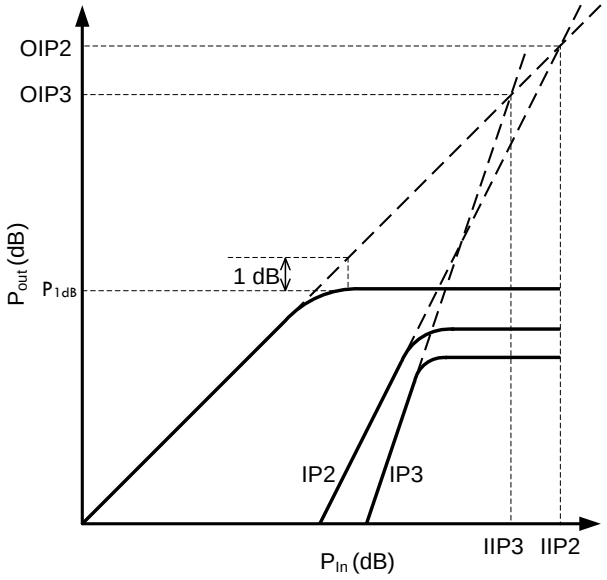


Figure 2.14: Intercept points.

2.2.5 Figures of Merit for LNAs

In the literature it is common to find a variety of LNA designs, optimized for different parameters such as gain, noise figure, linearity, and power consumption. Even for similar topologies, the results can be quite different, depending on the optimization purpose. To compare these different designs, usually the most important parameters are included into a formula called figure of merit (FoM) in order to determine which design is more efficient. A popular FoM (2.25) is related the noise and gain performances, and is normalized to the power consumption [35].

$$FoM_1[mW^{-1}] = \frac{\text{Gain}}{(F-1)\cdot P_{DC}[mW]} \tag{2.25}$$

However, nothing can be concluded about the performance regarding the other parameters. In (2.26) a more complete FoM is presented, proposed in [36], that includes $IIP3$ and the frequency of operation f_C. This FoM is suitable for narrowband LNAs only, since the bandwidth is not considered.

$$FoM_2[-] = \frac{\text{Gain}\cdot \text{IIP3[mW]}\cdot f_c[\text{GHz}]}{(F-1)\cdot P_{DC}[\text{mW}]} \tag{2.26}$$

In order to have a fair comparison between wideband and narrowband LNAs , in [37] a FoM is proposed that includes the bandwidth and area, as follows:

$$FoM_3[dB] = 20\log\left(\frac{\text{Gain}\cdot \text{IIP3[mW]}\cdot BW[\text{GHz}]}{(F-1)\cdot P_{DC}[\text{mW}]\cdot A[mm^2]}\right) \tag{2.27}$$

2.3 Basic LNA Circuits

In this section, typical LNA specifications and LNA circuits are discussed.

The LNA, is typically the first amplifying stage. The LNA input impedance should match the antenna characteristic impedance to maximize the power transfer. The LNA should provide enough gain in order to minimize the overall influence of noise contribution from the subsequent stages, but the gain should not be too high, since large interferer signals that may have not been properly filtered at the input can saturate the following stage (e.g. mixer); in practice, a reasonable range of voltage gain is between 12 and 20 dB.

The noise factor should be the lowest possible to minimize the noise in the system, since the noise contribution of the first stage in a cascaded system is dominant, and besides the noise figure specifications could differ for different applications, a reasonable value usually adopted for the noise figure is below 3 dB.

As to LNA circuits, there are four basic approaches according to the input impedance matching, as described in the following [38].

2.3.1 Common-Source LNA with Inductive Degeneration

The CS LNA with inductive degeneration is one of the most used topologies to design a narrowband LNA, because it allows low noise figure, high gain, and easy input matching. The CS LNA shown in Fig. 2.15 is intrinsically narrowband since

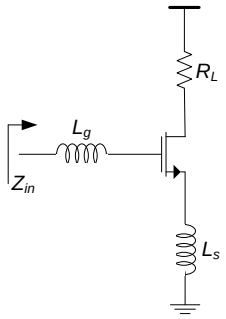


Figure 2.15: Common-Source LNA with inductive degeneration.

its input impedance is

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}} L_s \tag{2.28}$$

and the inductances L_s and L_g are chosen to resonate with the device capacitance C_{gs} at the frequency of operation

$$\omega_0 = \frac{1}{\sqrt{(L_g + L_s)C_{gs}}} \tag{2.29}$$

This eliminates the imaginary part of Z_{in} and the term $\frac{g_m}{C_{gs}} L_s$ is set to 50 Ω. The inductance L_g gives a degree of freedom in the LNA design, since the gain is proportional to g_m. The use of inductors, which are ideally noiseless, allow this topology to have one of the best noise performances, but it increases significantly the die area of the LNA. A major drawback is that RF options (thick metal layer)

needed to design high Q inductors , and the large die area, increase the production cost.

2.3.2 Common-Source LNA with Resistive Input Matching

The simplest way to obtain a stable wideband input impedance is to use resistive input matching. The CS stage, shown in Fig. 2.16, has a resistor is in parallel with the amplifier input. However, this resistor introduces a significant amount of noise.

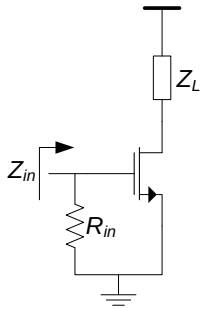


Figure 2.16: Common-Source stage with resistive input matching.

Assuming that the amplifier has an available power gain A_p and a noise power at the output P_n, due to internal sources only, if the source has an impedance R_S, the noise factor can be expressed by:

$$F = \frac{Total\ output\ noise}{Total\ output\ noise\ due\ to\ input\ source}$$

$$= \frac{4kTR_SA_p + 4kTR_{in}A_p + P_n}{4KTR_SA_p} = 2 + \frac{P_n}{4KTR_SA_p} \tag{2.30}$$

which establishes a minimum noise figure of 3 dB, which is a high value for some applications.

2.3.3 Common-Gate LNA

The common-gate topology (Fig. 2.17) has an intrinsic wideband response, which is one of the reasons why it is widely used to implement LNAs. In a first order analysis, its input impedance is approximately $\frac{1}{g_m}$, and g_m can be easily dimensioned to achieve the input impedance matching.

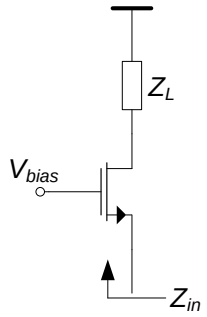


Figure 2.17: Common-Gate LNA.

To estimate the lower bound of the noise factor, only the transistor thermal noise is considered. If it is referred to the input, we obtain [38]:

$$F = 1 + \gamma g_{d0} R_S = 1 + \frac{\gamma}{\alpha} g_m R_S \tag{2.31}$$

where $\alpha \approx \frac{g_m}{g_{d0}}$. For long channel devices, the noise excess factor γ[1] is $\frac{2}{3}$ and the short-channel effects can be neglected ($\alpha = 1$) [29], [30]. For input matching, $g_m R_S = 1$. Thus, the minimum noise factor is about $F = \frac{5}{3}$, which corresponds a noise figure of 2.2 dB.

The CG-LNA has a disadvantage: since g_m is imposed by the matching condition, the gain is only dependent on the load Z_L. Increasing Z_L increases the gain, but also increases the noise. This limits the gain that it is possible to achieve. In practice, the CG-LNA has typical noise figure values above 3 dB.

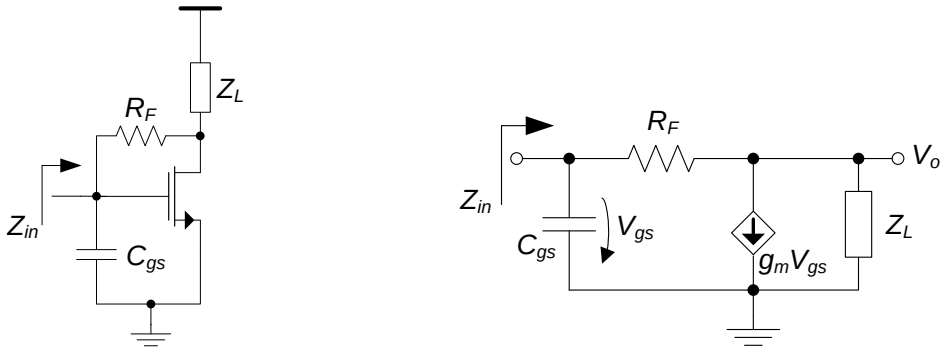
2.3.4 LNA with resistive shunt feedback

The wideband LNA represented in Fig. 2.18(a) uses the feedback resistor R_F. Using the incremental model (Fig. 2.18(b)), the input impedance is:

$$Z_{in} = \frac{R_F + Z_L}{sC_{gs}(R_F + Z_L) + 1 + g_m Z_L} = \left(\frac{1}{sC_{gs}} // \frac{R_F + Z_L}{1 + g_m Z_L} \right) \tag{2.32}$$

which depends on many parameters, so, for the sake of simplicity, some assumptions will be made. For frequencies such that C_{gs} is negligible, the gate is seen as a high impedance, and assuming that $Z_L >> R_F$ the input impedance simplifies to $1/g_m$.

[1]This value is often empirically determined and can be higher for short channel devices, between 1 and 3.



(a) (b)

Figure 2.18: LNA with resistive shunt feedback: (a) schematic (b) small signals model for low and medium frequencies.

Using a similar analysis for low frequencies, the gain is:

$$A_v = \frac{(1 - g_m R_F) Z_L}{R_F + Z_L} \tag{2.33}$$

and if the load Z_L is high and $g_m R_F >> 1$, the gain is simplified to:

$$A_v \approx -g_m R_F \tag{2.34}$$

This approximation is useful when considering the noise factor, that is found to be [39]:

$$F = 1 + \frac{R_F}{R_S}\left(\frac{1 + g_m R_S}{1 - g_m R_F}\right)^2 + \frac{1}{R_S Z_L}\left(\frac{R_F + R_S}{1 - g_m R_F}\right)^2 + \frac{\gamma g_m}{\alpha R_S}\left(\frac{R_F + R_S}{1 - g_m R_F}\right)^2 \tag{2.35}$$

At first sight, by increasing the term $g_m R_F$, the noise factor is reduced and the gain is enhanced, as intended. According to the previous assumptions for gain and noise optimization, g_m is set by the input matching condition, and R_F must be increased. However if the load Z_L becomes comparable to R_F, then the previous assumptions are no longer valid. Thus, g_m and R_F have to be carefully dimensioned to achieve an optimal performance.

CHAPTER 3

STATE-OF-THE ART WIDEBAND LNAS

Recently there has been a proliferation of wireless communication standards that cover a wide range of the spectrum, from tens of MHz up to several GHz. This has led to the development of multi-standard radio architectures capable of handling the stringent specifications of the standards. With this in mind, two approaches to multi-standard RF front-ends are possible, one using several dedicated narrow-band LNAs covering the specific target bands and the other by employing a single wideband LNA. The first approach has the advantage that narrowband LNAs are known to achieve better performance, particularly very low noise figures, but it increases the circuit complexity and the production cost is high, due to the large area occupied. Wideband LNAs have larger noise figure than narrowband LNAs, but are simpler and typically have lower power consumption and cost. Therefore, their use have become very popular which motivated much of the research effort in wideband LNAs, in order to obtain reasonable noise figures.

This chapter is devoted to present a review of state-of-the art wideband LNAs.

3.1 Balun LNA with Noise and Distortion Cancellation

The LNA in Fig. 3.1 published in 2008 [8] is one of the most significant state-of-the-art inductorless LNAs. This circuit is particularly attractive because it combines a CG stage and a CS stage, performing a balun (single ended to differential) conversion and it allows noise and distortion cancellation; this is very advantageous, since the LNA is, typically, preceded by a filter or is directly coupled to an antenna, which have a single output (there are antennas with differential outputs, but these are not common in on-chip RF front-ends), is simpler to use an LNA with a single-ended input. Since the subsequent stage (e.g, mixer) usually has differential inputs, a balun is required in the case of a single ended LNA. A passive wideband balun has high losses, and a low loss balun is mainly narrowband and must be implemented externally.

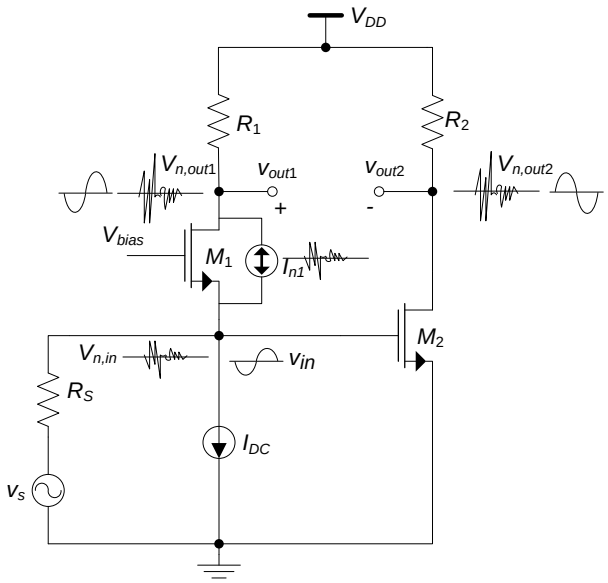


Figure 3.1: Inductorless Balun LNA.

Balun Operation

Analysing the circuit of Fig. 3.1 and assuming ideal transistors with infinite output resistance, all the input current flows into the CG stage through R_1 originating

the output signal V_{out1} which has the same phase as v_{in}, and the gain Av_{CG} is roughly given by $g_{m1}R_1$. The input impedance Z_{in} is set by the CG stage, which is approximately $1/g_{m1}$, and has to be equal to R_S for ideal input matching. For proper balun operation both stages must have equal gains with opposite output signs for differential operation. The CS stage has a gain Av_{CS} approximately given by $-g_{m2}R_2$. Thus:

$$Av_{CG} = -Av_{CS} = \frac{R_1}{R_S} \tag{3.1}$$

Noise and Distortion Cancellation

The thermal noise produced by the CG stage (M_1), represented by the current source I_{n1}, originates a noise voltage at the input $V_{n,in}$ since it flows into R_S. This generates noise voltages in opposition at the CG output $V_{n,out1}$ and at the CS output $V_{n,out2}$. Thus, the CG thermal noise is cancelled and the gain is doubled at the differential output. The gain matching of the two stages is critical, since the same gain is needed for full noise cancellation.

This structure also allows the cancellation of the distortion introduced by the CG stage. Transistor M_1 originates a nonlinear current i_{ds} which is dependent on the two incremental voltage variations v_{gs} and v_{ds}, and it flows through the linear resistor R_S originating a nonlinear voltage at the input v_{in}.

This voltage can be represented as a function of v_s by a Taylor expansion:

$$v_{in} = \alpha_1 v_s + \alpha_2 v_s^2 + \alpha_3 v_s^3 + \cdots + \alpha_n v_s^n = \alpha_1 v_s + v_{NL} \tag{3.2}$$

where the α_i are the Taylor coefficients and v_{NL} contains all the unwanted nonlinear voltages. Thus the voltage at the CG output can be expressed as:

$$v_{out1} = i_{in}R_1 = \frac{v_s - v_{in}}{R_S}R_1 = ((1-\alpha_1)v_s - v_{NL})\frac{R_1}{R_S} \tag{3.3}$$

and considering (3.1), the voltage at the CS output is:

$$v_{out2} = -v_{in}\frac{R_1}{R_S} = -(\alpha_1 v_s + v_{NL})\frac{R_1}{R_S} \tag{3.4}$$

Therefore, all the nonlinearities generated by the CG are cancelled as a result of the differential operation, remaining only a linear signal:

$$v_{out} = v_{out1} - v_{out2} = v_s \frac{R_1}{R_S} \tag{3.5}$$

For the noise factor calculation, the transistors are assumed to have infinite output impedance and the current source I_{DC} is assumed to be ideal. Moreover, only the thermal noise of the resistors and transistors are considered. With these assumptions, the noise figure is given by [8]:

$$F = 1 + \frac{\gamma g_{m1}(R_1 - R_S g_{m2} R_2)^2 + \gamma g_{m2} R_2^2 (1 + g_{m1} R_S)^2 + (R_1 + R_2)(1 + g_{m1} R_S)^2}{R_S A_v^2} \tag{3.6}$$

It is worth noting here that there is a tradeoff between power and noise figure, in order to reduce the overall noise figure. It can be seen by inspection of the second term of 3.6, that if R_2 is reduced and g_{m2} is incresead in the same proportion to achieve the same gain for proper noise cancellation, the noise factor is reduced. However the increase of the transconductance implies a significant increase of the bias current in the CS stage or in the transistor M_2 W/L ratio and consequently area.

3.2 Wideband LNA with Local Feedback and Noise Cancellation

Unlike in digital circuits design, in which the supply voltage tends to scale down with the technology, in RF analog circuit design it is preferable to have a higher supply voltage to achieve higher gain and better linearity. However, this could be critical due to the low breakdown voltage of sub-micron CMOS technology. Moreover, in inductorless designs, the resistors require extra voltage drops, which is a constraint in analog design. The LNA in Fig. 3.2 is also based on the CG-CS topology and introduces a local negative feedback between the CG and CS stages, to allow a low-voltage and low power design to overcome the aforementioned limitations [40].

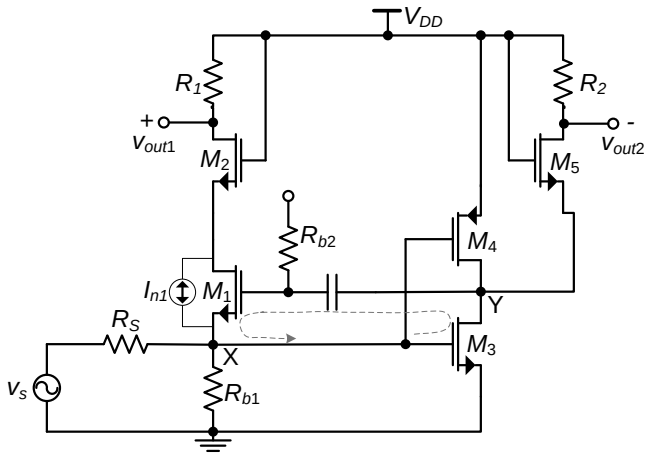


Figure 3.2: LNA with Negative Feedback.

The principle of operation for noise cancellation is the same of the previous balun LNA. The noise generated by M_1 appears with phase opposition at the output v_{out1} and at the input node X. The pair M_3 and M_4 behaves as a CMOS inverter based amplifier, so the input signal is inverted at node Y and amplified to the output v_{out2}.

For proper impedance matching, one must satisfy the following condition:

$$R_S = \frac{1}{g_{m1}(1 + A_{vY})} \tag{3.7}$$

where A_{vY} is the voltage gain from node X to node Y. M_1 benefits from gain boosting due to the local feedback loop, therefore it's transconductance g_{m1} can be reduced by a factor $1 + A_{vY}$, giving an additional degree of freedom to optimize the noise figure.

If the input matching condition is satisfied, the gain can be simplified to:

$$A_v = \frac{R_1}{R_S} + (g_{m3} + g_{m4})R_2 \tag{3.8}$$

and to obtain a balanced differential output and simultaneously noise cancellation the, following condition must be satisfied:

$$\frac{R_1}{R_S} = (g_{m3} + g_{m4})R_2 \tag{3.9}$$

Therefore, the voltage gain can be rewritten as:

$$A_v = 2(g_{m3} + g_{m4})R_2 \tag{3.10}$$

Under the conditions of impedance matching and output balance, the noise factor can be derived as [40]:

$$F = 1 + \frac{\gamma_3 g_{m3}}{\alpha_3 (g_{m3}+g_{m4})^2 R_S} + \frac{\gamma_4 g_{m4}}{\alpha_4 (g_{m3}+g_{m4})^2 R_S} + \frac{1}{R_S (g_{m3}+g_{m4})^2 R_2} + \frac{R_S}{R_{b1}} + \frac{R_S}{R_1} + \frac{\gamma_5}{\alpha_5 4 R_S g_{m5} (1+A_{vY})^2}\epsilon_m^2 + \frac{\gamma_1}{\alpha_1 4 (1+A_{vY})}\epsilon_m^2 \tag{3.11}$$

where ϵ_m^2 represents the gain imbalance of the differential output due to mismatches. If the two stages have the same gain, the last two terms of (3.11) can be neglected. The second and third terms refer to noise contribution of transistors M_3 and M_4, which are the major noise contributors.

3.3 Wideband LNA with Composite Transistor Pairs and Noise Cancellation

The two LNAs mentioned above employ noise cancellation techniques, that require precise matching between devices to achieve an effective noise cancellation and, thus, a significant noise figure reduction. The LNA in Fig. 3.3 uses a composite NMOS/PMOS transistor pairs connected in a cross coupled configuration, which provides a partial cancellation of the noise generated by the NMOS transistors [41].

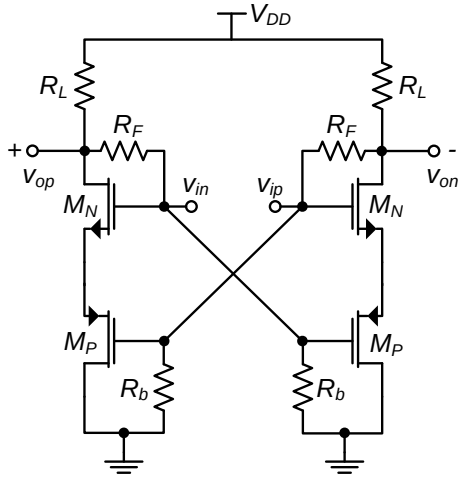
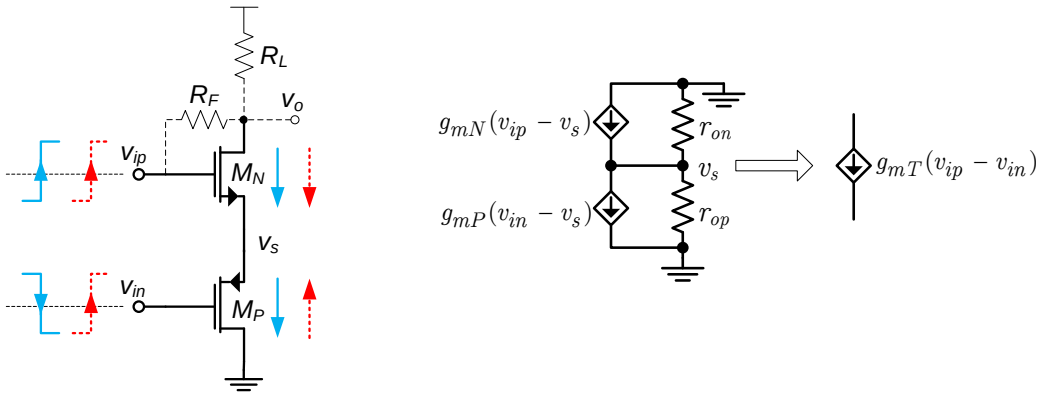


Figure 3.3: Wideband LNA with Composite Transistor Pairs.

Principle of operation

To understand the principle of operation, the basic core cell of the LNA is represented in Fig. 3.4(a) in solid lines. In this configuration, the NMOS/PMOS pair appears in series and it is supposed to have a differential mode input. From a first inspection of the circuit, assuming that both signals have the same amplitude and phase, when the signal is rising around a fixed DC bias point, the NMOS overdrive voltage ($v_{ip} - v_s$) is rising and the current increases, but the overdrive voltage of PMOS ($v_{in} - v_s$) is decreasing and in that case the current is flowing in the opposite direction; therefore, the two incremental currents cancel each other. In the other situation where the input signals are in phase opposition the current flows in the same direction in both transistors.



(a) (b)

Figure 3.4: (a) NMOS/PMOS cell (b) small signal model.

In Fig. 3.4(b) the equivalent small signal model is represented. For the case where signals are in opposition, the following relation is obtained from the small signal analysis:

$v_{id} = v_{ip} - v_{in}$ where $v_{ip} = \frac{v_{id}}{2}$ and $v_{in} = -\frac{v_{id}}{2}$:

$$g_{mN}(v_{ip} - v_s) - g_{mP}(v_s - v_{in}) - v_s(r_{op}//r_{on}) = 0 \Leftrightarrow$$

$$\frac{v_s}{v_{id}} = \frac{g_{mN} - g_{mP}}{2(g_{mN} + g_{mP} + g_{oN} + g_{oP})} \approx 0 \tag{3.12}$$

which leads to v_s as virtual ground originating an output finite current. On the other hand if both signals are in phase, then:

$v_i = v_{ip} = v_{in}$:

$$\frac{v_s}{v_i} = \frac{g_{mN} + g_{mP}}{g_{mN} + g_{mP} + g_{oN} + g_{oP}} \approx 1, \; for \; g_{mN} + g_{mP} >> g_{oN} + g_{oP} \tag{3.13}$$

and in this case v_s has approximately the same amplitude of the input signal, confirming that no current is flowing through the transistors. Thus, one can conclude that in this configuration the differential input signal is amplified and the common mode is rejected, and this composite pair can be simplified and represented by its effective transconductance g_{mT}:

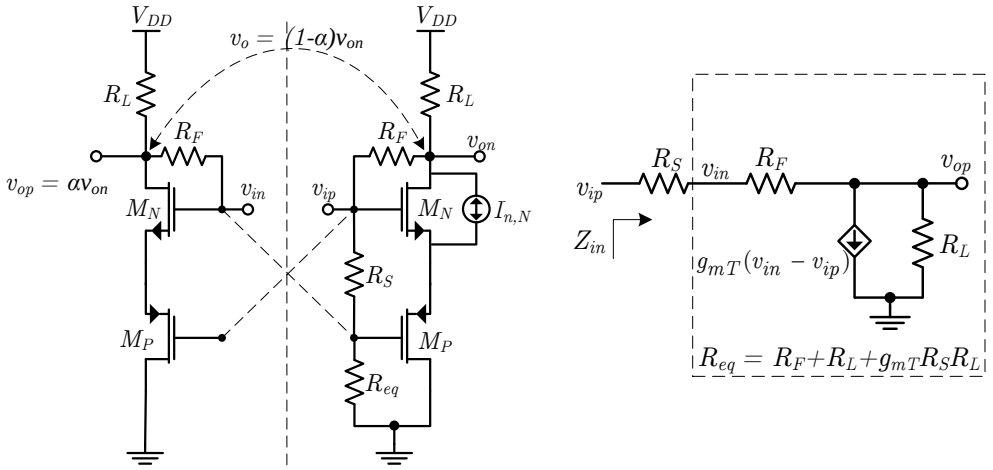
$$g_{mT} = \frac{i_d}{v_{id}} = \frac{g_{mN} g_{mP}}{g_{mN} + g_{mP}} \tag{3.14}$$

From a noise perspective, the cross connection allows a partial cancellation of the noise generated by the transistors. This can be shown qualitatively by inspection of the circuit, considering the noise generated by one of the transistors. As depicted in Fig. 3.5(a), the noise introduced by the NMOS transistor of the circuit's right hand side is considered, and the left part of the circuit is represented by its equivalent input impedance as shown in Fig. 3.5(b), where the resistance R_S of the power source is considered.

The current noise generated by the transistor originates a voltage noise at the output node v_{on}, which at the same time produces a current noise flowing through the resistors originating a noise voltage at the nodes v_{ip} and v_{in} that drive the left-hand side transistors, producing an output noise v_{op} which happens to be a fraction α of v_{on}. Since both, v_{op} and v_{on} have the same polarity, then a fraction of the noise is cancelled when performing the subtraction from the differential operation. The same analysis can be done for the PMOS transistors, and exploiting this partial noise cancellation the overall noise figure can be reduced.

The gain is given by:

$$A_v = \frac{V_{op} - v_{on}}{V_{in} - V_{ip}} \approx 2 g_{mT} (R_F // R_L) \tag{3.15}$$



(a) (b)

Figure 3.5: Equivalent circuit model showing partial noise cancellation: (a) Effect of noise current generated by M_N (b) Equivalent input impedance from the left-hand side of the circuit.

and the input impedance is given by:

$$Z_{in} = 2\frac{R_F}{1+A_v} \approx \frac{1}{g_{mT}}\left(1+\frac{R_F}{R_L}\right) \tag{3.16}$$

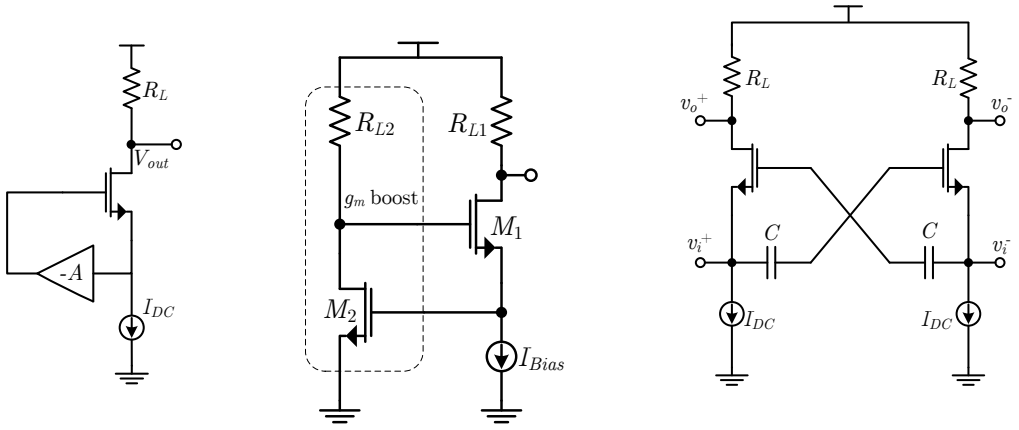
The noise factor can be derived as [41]:

$$F = 1 + \frac{\gamma_N}{2R_S g_{mN}} + \frac{\gamma_P}{2R_S g_{mP}} + \frac{\left(\frac{K_{fN}}{g_{mN}^2 L_N^2} + \frac{K_{fP}}{g_{mP}^2 L_P^2}\right) I_{DC}}{8kTfC_{ox}R_S} + \frac{1}{2}\left(1+\frac{1}{g_{mT}R_S}\right)^2 \frac{R_S}{R_F} + \frac{1}{2g_{mT}^2 R_L R_S} \tag{3.17}$$

3.4 Wideband LNA with Double G_m Enhancement

All the LNAs mentioned above employ noise cancellation techniques to achieve lower noise figures than conventional wideband LNAs. The LNA considered now uses g_m boost techniques and is targeted for low power applications. The basic idea behind the g_m boosting, shown in Fig. 3.6(a), consists of the application of a signal at both source and gate of a MOS transistor in phase opposition, in order to increase the gate-source voltage v_{gs} and consequently the effective transconductance g_m. It can be seen that when an inverting gain is inserted between

gate and source terminals, the effective g_m is increased to $(1+A)g_m$. This technique has been widely used in CG LNAs [42], [43], mainly because it provides higher bandwidth, linearity and more insensitivity to PVT variations when compared to a CS topology [44]. In CG LNA design, the transconductance is restricted due to the input impedance matching which sets the limits to both gain and noise figure. The g_m boosting technique applied to a CG topology, gives a new degree of freedom and the design is no longer restricted by the MOS transistor transconductance.



(a) (b) (c)

Figure 3.6: G_m boost techniques: (a) g_m boosted CG stage (b) CS based g_m boost (c) capacitive cross-coupling based g_m boost.

One possible way to implement the inverting gain A, is by using a capacitive cross-coupling technique (CCC), as depicted in Fig. 3.6(c), where the inversion is inherently provided by the capacitors in a differential structure [45]. Due to the CCC technique, the effective transconductance is doubled, so the input transistor's transconductance can be reduced which enables a reduction in the current, as well the channel noise of the input devices. Moreover, the CCC causes a common-mode noise voltages at the drain of the transistors which can be further reduced or ideally eliminated. However, since the gain A is based on passive elements it is limited to 1, but there are other alternatives employing an active amplifier. A common solution, is to use a CS stage as an auxiliary amplifier (Fig. 3.6(b)) which provides an inverting gain but requires additional power, in contrast with CCC technique.

The LNA proposed in [37] shown in Fig. 3.7 overcomes the matching and power

tradeoff, and simultaneously focuses on the power optimization by employing g_m boost in the auxiliary amplifier, thus doubles the effect of g_m boosting.

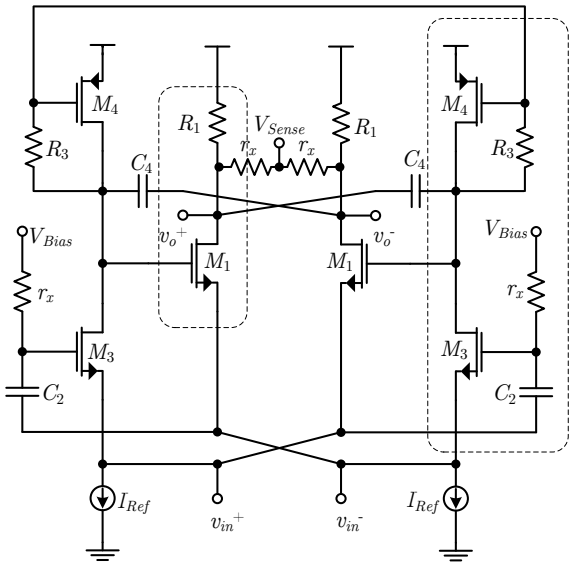


Figure 3.7: Wideband LNA with Double G_m Enhancement

The proposed circuit has a main CG amplifier, composed of M_1 and R_1, whose output is boosted by an auxiliary CG amplifier (M_3, R_3) instead of a CS stage, which is also boosted by a CCC technique (C_2). In this configuration the boosting gain is doubled ($G_B \approx 2g_{m3}R_3$) without requiring extra power consumption. Moreover, the finite input impedance of M_3 gives an extra degree of freedom to set the LNA input impedance. The capacitors C_4 are used for an extended bandwidth while the active loads (M_4) avoid the large DC voltage drops across R_3.

In Fig. 3.8 a simplified schematic is represented which is used to determine the low frequency input impedance, and the transistor's output conductances are neglected for simplicity.

From the schematic it is possible to obtain the following equations for voltages

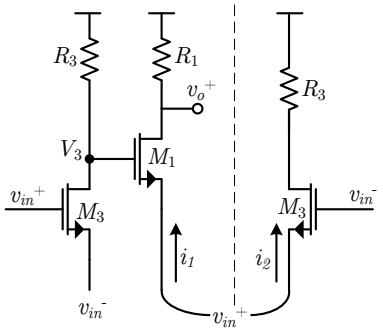


Figure 3.8: Partial circuit schematic used to determine the input impedance.

and currents:

$$\begin{cases} v_{id} = v_{in}^+ - v_{in}^- \,;\, v_{in}^+ = \dfrac{v_{id}}{2}, v_{in}^- = -\dfrac{v_{id}}{2} \\ i_{in} = i_1 + i_2 = -(g_{m1}v_{gs1} + g_{m3}v_{gs3}) \\ v_{gs1} = v_3 - v_{in}^+ \\ v_{gs3} = v_{in}^+ - v_{in}^- = v_{id} \\ v_3 = g_{m3}R_3(1+A)v_{in}^- = -v_{id}g_{m3}R_3 \ (for A \approx 1) \end{cases} \tag{3.18}$$

It is important to notice here that the gain A is due to the coupling capacitor and therefore the gain of auxiliary amplifier is boosted to the double. From 3.18 we can relate all the voltages to v_{id} and obtain the input admittance Y_{in}, as follows:

$$\begin{aligned} i_{in} &= -\left(g_{m1}\left(-v_{id}g_{m3}R_3 - \frac{v_{id}}{2}\right) - v_{id}g_{m3}\right) \Leftrightarrow \\ Y_{in} &= \frac{i_{in}}{v_{id}} = g_{m1}\left(g_{m3}R_3 + \frac{1}{2}\right) + g_{m3} = \frac{g_{m1}}{2}(\underbrace{2g_{m3}R_3}_{G_B} + 1) + g_{m3} \end{aligned} \tag{3.19}$$

A simplified matching condition can be defined to set the transconductance of the main amplifier transistor (M_1), as follows:

$$g_{m1} = \frac{2(1 - g_{m3}R_S)}{R_S(1 + 2g_{m3}R_3)} \tag{3.20}$$

For a more realistic approach to the low frequency gain, the transistor's finite output resistances are considered, resulting in:

$$A_v = \frac{g_{m1}R_1}{1 + g_{ds1}R_1}\left(1 + \frac{g_{ds1}}{g_{m1}} + G_B\right) \tag{3.21}$$

where, the boosting factor G_B is replaced by:

$$G_B = \frac{(2g_{m3} + g_{ds3})R_3}{1 + g_{ds3}R_3} \tag{3.22}$$

In order to obtain a simplified equation for the noise factor, some assumptions are made. First, it is stated that the noise sources of both half-circuits are uncorrelated and only the transistor and resistor's thermal noise sources are considered. Thus, the contribution of each noise source, M_3, R_3, M_1, R_1, is separated by terms in the complete noise factor equation [37]:

$$F = 1 + \frac{\gamma_3}{2g_{m3}R_S} + \frac{1}{2g_{m3}^2R_3R_S} + \frac{2\gamma_1}{g_{m1}R_S(1+G_B)^2} + \frac{2\left(1 + g_{m1}R_S\left(1 + \frac{G_B}{2}\right)\right)^2}{g_{m1}^2R_1R_S(1+G_B)^2} \tag{3.23}$$

where it is assumed that $G_B = 2g_{m3}R_3$, $2R_3 >> R_S$, $2g_{m3}R_3 >> 1$ and $g_{m1,3}R_S << 1$. From 3.23, it can be qualitatively concluded that M_3 and R_3 are the main noise contributors.

3.5 Discussion

To conclude this literature review, the equations for the relevant performance parameters are summarized in Table 3.1. It is worth mentioning that, of the many LNA designs available in the literature, those described in this chapter deserve special attention for their relevance in the context of this thesis, since they are wideband and use noise and distortion cancellation, and show the trends and evolution over the past five years.

Table 3.1: Summary of the LNAs parameters.

LNAs	[8](JSSC'08)	[40] (TCAS-I'10)	[41] (JSSC'11)	[37] (JSSC'12)
Z_{in}	$\frac{1}{g_{m1}}$	$\frac{1}{g_{m1}(1+A_{vY})}$	$\frac{1}{g_{mT}}\left(1+\frac{R_F}{R_L}\right)$	$\frac{2}{g_{m1}(1+2g_{m3}R_3)+2g_{m3}}$
Matching Condition	$g_{m1}=\frac{1}{R_S}$	$g_{m1}=\frac{1}{R_S(1+A_{vY})}$	$g_{mT}=\frac{1}{R_S}\left(1+\frac{R_F}{R_L}\right)$	$g_{m1}=\frac{2(1-g_{m3}R_S)}{R_S(1+2g_{m3}R_3)}$
Voltage Gain	$g_{m1}R_1+g_{m2}R_2$	$2(g_{m3}+g_{m4})R_2$	$2g_{mT}(R_F//R_L)$	$\frac{g_{m1}R_1}{1+g_{ds1}R_1}\left(1+\frac{g_{ds1}}{g_{m1}}+G_B\right)$
Noise Figure	(3.6)	(3.11)	(3.17)	(3.23)

Based on the techniques employed, it becomes evident that these circuits have in common the noise cancellation, gain boosting or a combination of both techniques. The advantages and disadvantages of each circuit are summarized in Table 3.2.

Table 3.2: Comparison of LNAs tradeoffs.

LNA	Advantages	Disadvantages
[8](JSSC'08)	✔ balun operation ✔ circuit simplicity ✔ noise and distortion cancellation ✔ good linearity ✔ wide bandwith	✖ high sensitivity to dc bias variation ✖ sensitivity to PVT variations ✖ limited gain
[40] (TCAS-I'10)	✔ balun operation ✔ low voltage operation ✔ low power ✔ flexible design	✖ reduced bandwidth ✖ linearity dependence on dc bias variations
[41] (JSSC'11)	✔ partial noise cancellation ✔ very low noise figure ✔ good linearity	✖ differential input ✖ limited bandwidth ✖ high power consumptiom ✖ circuit complexity
[37] (JSSC'12)	✔ high voltage gain ✔ very low power	✖ differential input ✖ circuit complexity ✖ limited bandwidth ✖ poor linearity

In this thesis we expect to achieve a LNA design that maintains the key advantages of the above circuits and alleviates some of the disadvantages (e.g., circuit

complexity, linearity and sensitivity to PVT variations).

CHAPTER 4

LNA WITH ACTIVE LOADS

4.1 Introduction

This chapter presents the study of a single-ended input LNA, which combines the balun and LNA functionalities in order to obtain a simple and low cost LNA.

In the design of a wideband LNA there is an important choice to be made. A single-ended input simplifies the connection to the antenna and RF filters (they are usually single-ended) and avoids the need of a balun for the single to differential conversion (the balun usually has high loss and degrades the NF significantly). A differential circuit leads to reduced harmonic distortion and to better power supply and substrate noise rejection.

To achieve the main goal of this thesis, the design of a very low area and low-cost LNA, and at the same time with less circuit variability, a MOSFET-only approach is investigated which consists of implementing the resistors using transistors. As it will be shown, this approach adds a new degree of freedom, which can be used to maximize the LNA gain, and, therefore, minimize the circuit noise figure. In addition, this implementation allows a continuously controllable gain, with minimum impact on linearity, through the variation of the biasing of the MOSFET loads, which is a desirable feature in mobile RF devices.

A comparison of the proposed approach is presented with the conventional LNA using resistors, under the same bias conditions.

4.2 Proposed circuit

The proposed circuit is based on the conventional CG-CS architecture described in Chap. 3.1 (Fig. 3.1), where the passive loads are replaced by PMOS transistors, as shown in Fig. 4.1.

In modern CMOS processes, the polysilicon resistors have typically, an overall sheet resistance variation in the range of 15% to 25% [46], which can be critical if high accuracy is desired. The implementation with active loads allows the minimization of the circuit sensitivity to process variations. Besides this advantage, it is possible to achieve a higher value for the load under the same current bias in comparison with resistors, and also a higher dynamic range. However, it is expected an increase of noise, distortion and a reduced bandwidth due to the non-linear MOSFET characteristic and parasitic capacitances.

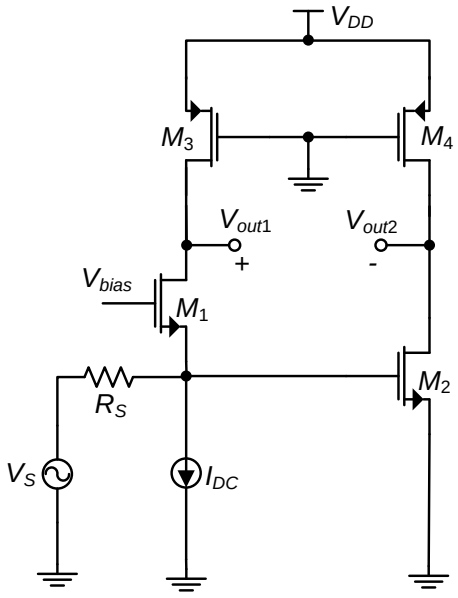


Figure 4.1: Proposed LNA with active loads.

4.3 Circuit Implementation

The PMOS transistors (M_3, M_4), if biased deeply in the triode region ($V_{DS} \ll V_{GS} - V_{th}$), can be ideally modeled by a resistor between the drain and source,

$$r_{ds} = \frac{1}{g_{ds}} \tag{4.1}$$

where g_{ds} is the channel conductance. The design procedure can be divided into three steps:

- Set g_m of transistor M_1 for 50 Ω input impedance matching. The bias current (I_{DC}) is set to a value compatible with the acceptable power consumption (2 mA in this design, as shown in Table 4.1), and the value of W is calculated assuming minimum L to maximize the circuit bandwidth.

- Consider the same current for the common-source stage (2 mA), to minimize the total power consumption, and obtain W of M_2, assuming minimum L. These values are slightly different from those of transistor M_1, since M_2 does not suffer from body effect.

- Optimize the value of the active loads in order to maximize the gain and reduce the NF, without degrading the input matching.

Once the resistors are replaced by MOSFETs it becomes possible to optimize the circuit gain. The incremental model of a MOS transistor operating in saturation is a current source in parallel with a resistor. The incremental load resistance can be increased with a lower DC voltage drop in comparison with passive resistors, thus increasing the gain with respect to the original circuit with resistor loads. By simulation, the optimal gain point of the LNA can be found through the variation of $W = W_3 = W_4$ (with $L_3 = L_4 = L_{min}$). It is observed that the gains of the CG and CS stages increase until a point is reached for which the gains are no longer almost equal, and beyond that point the gains diverge, thus, violating the condition for noise and distortion cancellation. This is the optimal gain point, shown in Fig. 4.2. It is easy to see that the corresponding biasing is in triode, but not far from the saturation region.

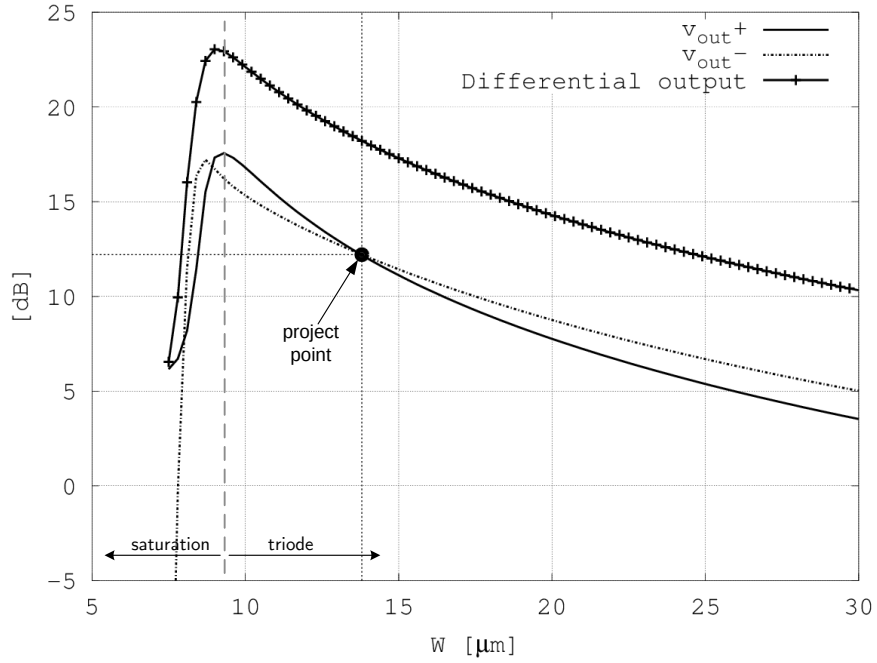


Figure 4.2: LNA optimum gain point.

The biasing and design parameters, for the circuit example, are summarized in Table 4.1.

Table 4.1: Circuit design values.

	I_D [mA]	g_m [mS]	W [µm]	L [µm]
M_1	2	25.1	75.6	0.12
M_2	2	26.1	77	0.12
M_3	2	2	13.8	0.12
M_4	2	2	13.8	0.12

* $V_{bias} = 895$ mV

Since M3 and M4 have the same aspect ratio and biasing voltage, their incremental resistances are equal, $r_{ds3} = rds4$, and the low frequency LNA gain is

$$A_{vLNA} = g_{m1}(r_{ds1}//r_{ds3}) + g_{m2}(r_{ds2}//r_{ds4}) \tag{4.2}$$

Comparing (4.2) with (3.1), it can be shown that a higher gain is achieved, since the value of $r_{ds3} = r_{ds4}$ is higher than $R_1 = R_2$ for the same bias conditions.

To achieve noise cancellation and balun operation the CG and CS's stages should be matched. Considering the circuit of Fig. 3.1 with resistive loads, and

assuming that gm1 = gm2 = gm (neglecting the body effect) and the loads $R_1 = R_2 = R_L$, if the flicker noise is taken into account, then the noise factor equation from (3.6) can be rearranged as:

$$F = 1 + \frac{k_f}{8kTR_S C_{ox} f^{\alpha f}} \left(\frac{1}{W_1 L_1} + \frac{1}{W_2 L_2} \right) + \frac{\gamma}{2R_S g_m} + \frac{1}{R_S R_L g_m^2} \tag{4.3}$$

where k is Boltzmann's constant, C_{ox} is the oxide gate capacitance per unite area, W_i and L_i are the transistor dimensions, T is the absolute temperature, γ is the transistors' excess noise factor, k_f and αf are intrinsic process parameters, which depend on the size of the transistors [47], [48]. In the case of the LNA with active loads, besides the thermal noise, the flicker noise due to transistors M_3 and M_4 must also be taken into account, and since it is assumed that $r_{ds3} = r_{ds4} = r_{ds}$, from (4.3) the noise factor is:

$$\begin{aligned} F = 1 + \frac{k_f}{8kTR_S C_{ox} f^{\alpha f}} \left(\frac{1}{W_1 L_1} + \frac{1}{W_2 L_2} + \frac{1}{W_3 L_3} + \frac{1}{W_4 L_4} \right) \\ + \frac{\gamma}{2R_S g_m} + \frac{1}{R_S r_{ds} g_m^2} \end{aligned} \tag{4.4}$$

Comparing Eq. (4.4) with Eq. (4.3), it is clear that the noise at low frequencies will be higher, but the last term of Eq. (4.4) is lower since r_{ds} is higher than R_L for the same voltage drop across the resistance. Thus, the noise figure can be reduced without changing the value of g_m, without any penalty in terms of area and power dissipation.

4.4 Gain variability and distortion analysis

It has been shown how the proposed MOSFET-only LNA can be optimized for maximum gain and low NF, but with a small modification in the original circuit, it will be demonstrated how it can be more flexible by allowing a continuously controllable gain while minimizing the impact of distortion due the MOSFETs non-linearities. Fig. 4.3 shows the modified version of the LNA. The voltage gain is controlled by V_{tune}, and the effect of bias current differences on the circuit performance is reduced by using two biasing voltages, V_{B1} and V_{B2}, with a high pass

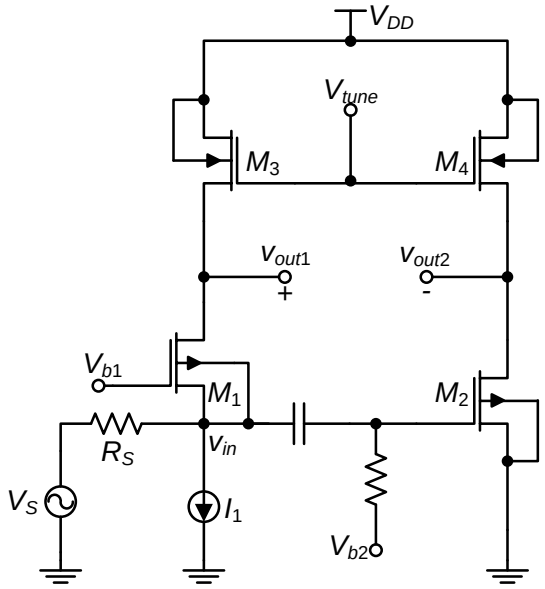


Figure 4.3: Proposed LNA with variable gain.

RC coupling. The bulk and source of M_1 are connected to suppress the body effect, which would deteriorate the performance due to the reduced noise cancellation. The reason why it was chosen not to benefit from the body effect in the design, is that the gain matching of the two stages is critical, and since the gain is desired to be continuously controllable, the circuit could only be optimized for one situation where the gain would be equal for both stages.

Distortion analysis

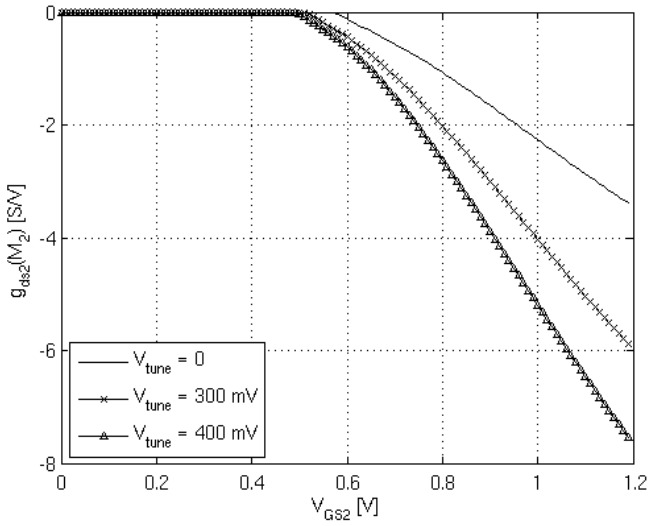
Since the resistors have been replaced by non-linear devices, suitable linearity of the LNA should be ensured for all the gain range. It is investigated how to improve the linearity by a proper biasing. The non-linearity of the CS stage (M_2, M_4) is of special concern, since the distortion of the CG stage can be cancelled out. The transistor current equation can be represented by a Taylor series expansion as a function of v_{gs} and v_{ds} [8], [40]:

$$\begin{aligned} id(v_{gs}, v_{ds}) = {} & g_{m1}v_{gs} + g_{ds1}v_{ds} + g_{m2}v_{gs}^2 + g_{ds2}v_{ds2}^2 + g_{11}v_{gs}v_{ds} + g_{m3}v_{gs}^3 \\ & + g_{12}v_{gs}v_{ds}^2 + g_{21}v_{gs}^2v_{ds} + g_{ds3}v_{ds}^3 \end{aligned} \tag{4.5}$$

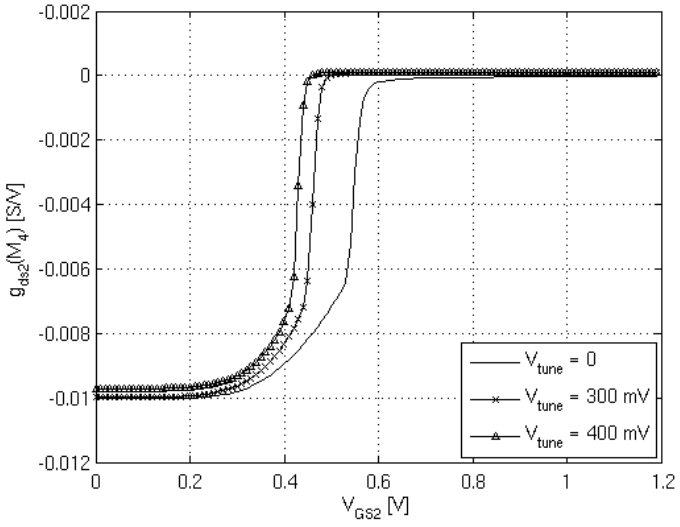
where,

$$g_{mk} = \frac{1}{k!}\frac{\partial^k i_{DS}}{\partial v_{GS}^k}, \quad g_{dsk} = \frac{1}{k!}\frac{\partial^k i_{DS}}{\partial v_{DS}^k}, \quad g_{jk} = \frac{1}{j!k!}\frac{\partial^{j+k} i_{DS}}{\partial v_{GS}^j \partial v_{DS}^k}$$

In small signal analysis, M_4 has $v_{gs} = 0$, because the gate is connected to a fixed DC voltage and, consequently, the distortion originated by this transistor is only due to v_{ds}. In Figs. 4.4(a) and 4.4(b) the simulated second order coefficients of M_2 and M_4, as a function of V_{GS} of M_2, are compared for different biasing of M_4, thus, different loads.



(a)



(b)

Figure 4.4: Second order coefficients (g_{ds2}) for: (a)transistor M_2 (b)transistor M_4.

The coefficient g_{ds2} of M_2 is more than 100 times higher than g_{ds2} of M_4, and

the difference is even higher for the third order coefficients, as it was confirmed by electrical simulations. Thus, M_4 does not introduce significant distortion, and it can be assumed that M_4 is simply modeled by a resistor r_{ds}. M_4 defines the CS stage gain, but its influence on IIP_2 and IIP_3 is negligible. This results from M_4 being in triode and not in saturation.

The output voltage of the CS stage is $v_{ds} = -i_d r_{ds}$, and it can be expressed as a non-linear function of v_{gs},

$$v_{ds} = -(c_1 r_{ds} v_{gs} + c_2 r_{ds} v_{gs}^2 + c_3 r_{ds} v_{gs}^3) \tag{4.6}$$

By substituting (4.6) in (4.5), i_d can be expressed as a function of only v_{gs}:

$$i_d = c_1 v_{gs} + c_2 v_{gs}^2 + c_3 v_{gs}^3 \tag{4.7}$$

where the coefficients are:

$$c_1 = \frac{g_{m1}}{1 + g_{ds1} r_{ds}} \tag{4.8}$$

$$c_2 = \frac{g_{m2} + g_{ds2} c_1^2 r_{ds}^2 - g_{11} c_1 r_{rds}}{1 + g_{ds1} r_{ds}} \tag{4.9}$$

$$\begin{aligned} c_3 = \Bigg[\Big(& g_{m3} + g_{12} c_1^2 r_{ds}^2 + 2 g_{ds2} c_1 c_2 r_{ds}^2 - g_{11} c_2 r_{ds} \\ & - g_{21} c_1 r_{ds} - g_{ds3} c_1^3 r_{ds}^3 \Big) \left(\frac{1}{1 + g_{ds1} r_{ds}} \right) \Bigg] \end{aligned} \tag{4.10}$$

Thus, the equation from 4.6 can be rearranged as:

$$v_{ds} = k_1 v_{gs} + k_2 v_{gs}^2 + k_3 v_{gs}^3 \tag{4.11}$$

where:

$$k_1 = -c_1 r_{ds} \tag{4.12}$$

$$k_2 = -c_2 r_{ds} \tag{4.13}$$

$$k_3 = -c_3 r_{ds} \tag{4.14}$$

For different M_2 bias, the transistor parameters in Eq. (4.5) are extracted by simulation, and k_1, k_2 and k_3 are obtained by using (4.12) to (4.14). The coefficient k_1 is the gain of the CS stage, and the bias of M_2 is chosen to minimize the distortion (coefficients k_2 and k_3) while the gain is set to an acceptable value.

4.5 Simulation Results

The value of g_{m1} of M_1 is set by the required 50 Ω input impedance (approximately equal to $\frac{1}{g_{m1}}$). Ideally, the transconductance of M_2 should be equal to that of M_1 for gain matching and noise cancellation; however, due to the loss of the RC network, the transconductance of M_2 should be slightly increased to reduce the noise figure.

The gain is set by an optimization procedure (Fig. 4.2), considering the maximum load, i.e.; when the PMOS transistors are close to saturation (e.g., $V_{tune} = 400$ mV, $V_{SG} = 800$ mV). As V_{tune} decreases until zero, the value of V_{dsat} increases turning the PMOS more into the linear region and consequently to a lower incremental resistance load.

The transistors widths are sized to $W_1 = 67.2$ μm, $W_2 = 92.8$ μm, and $W_3 = W_4 = 24$ μm. For maximum speed all transistors have the minimum channel length (120 nm). M_3 and M_4 were designed to have resistance between 90 Ω and 350 Ω, for V_{tune} from 0 to 400 mV. The bias voltage V_{B1} is 900 mV and V_{B2} is selected to improve the LNA linearity as explained below.

In Fig. 4.5 the coefficient k_1 in (4.12) is represented as a function of V_{GS} of M_2, which corresponds to the gain of CS stage for different load values of M_4. To maximize the gain, V_{GS} should be between 400 mV and 500 mV. In Figs. 4.6 and 4.7 the non-linearity coefficients k_2 and k_3 are shown. To minimize k_2 and k_3, V_{GS} should be below 400 mV for k_2 and bellow 450 mV for k_3. There is a trade off between gain and linearity: V_{GS} cannot be below 400 mV for a suitable gain, and cannot be more than 450 mV, for acceptable non-linearity. It can be concluded that a reasonable biasing range for M_2 is between 400 mV and 430 mV. Depending on the application, V_{GS} can be chosen to maximize the gain or to minimize IIP_3 and IIP_2. In this example a V_{GS} = 410 mV was chosen, which leads to a good overall

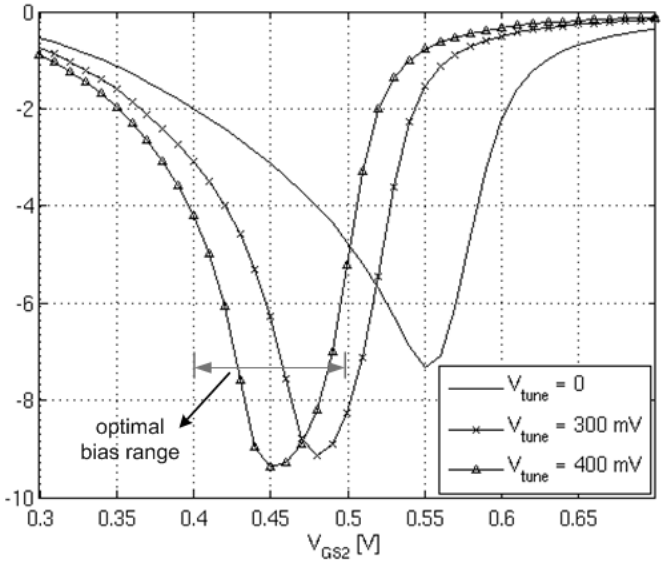


Figure 4.5: Coefficient k_1 as a function of V_{GS} of M_2.

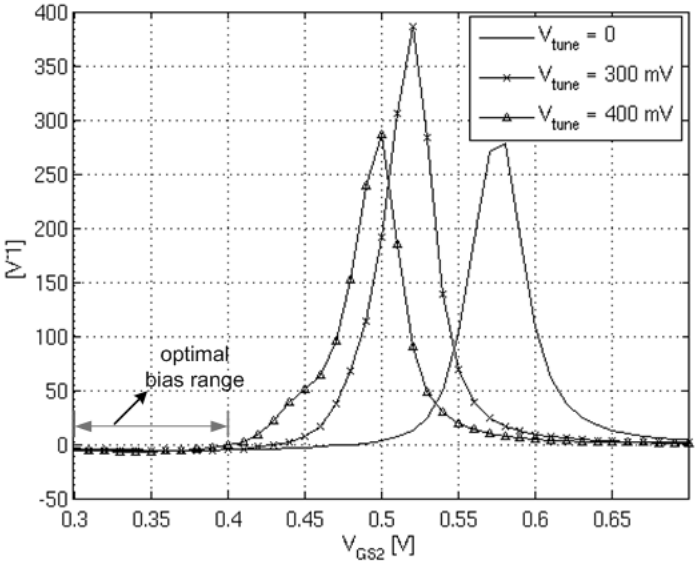


Figure 4.6: Coefficient k_2 as a function of V_{GS} of M_2.

LNA performance. The LNA gain and NF are shown in Figs. 4.8 and 4.9 for three different values of V_{tune}. The LNA performance is summarized in Table 4.2.

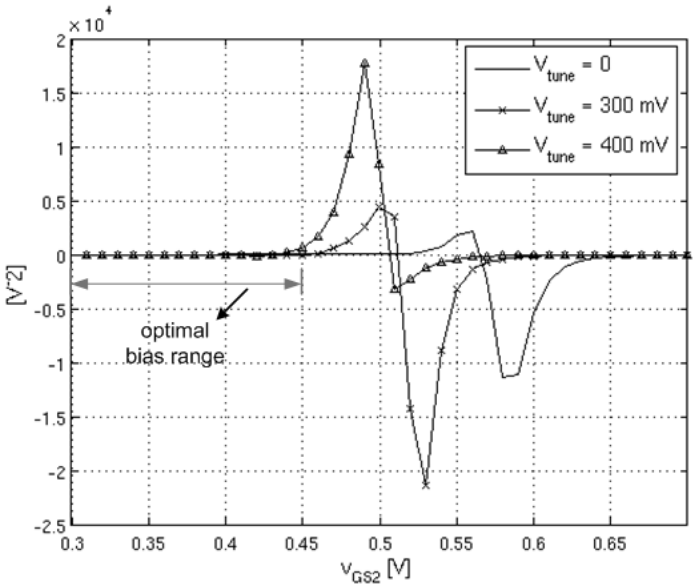


Figure 4.7: Coefficient k_3 as a function of V_{GS} of M_2.

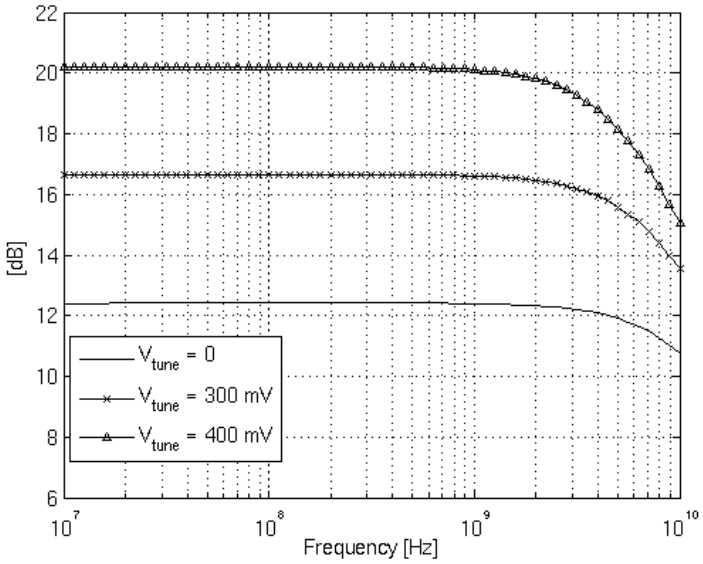


Figure 4.8: LNA Gain for three biasing voltages.

Table 4.2: LNA Performance.

V_{tune} [mV]	r_{ds} [Ω]	BW [GHz]	Gain [dB]	NF_{min} [dB]	IIP_2 [dBm]	IIP_3 [dBm]
0	90	10	12.4	3.2	6.2	0.7
300	170	8	16.6	2.7	14.4	-3.7
400	350	5	20.2	2.6	0	-10.9

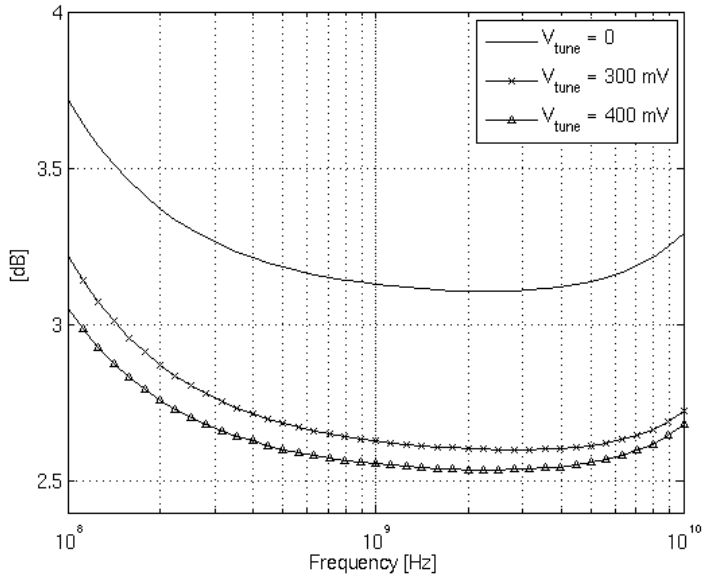


Figure 4.9: LNA NF for three biasing voltages.

4.6 Discussion and Conclusions

In this chapter, a wideband balun LNA with voltage-controlled continuously adjustable gain is presented. The key feature of this circuit is the replacement of the load resistors by PMOS transistors. With this simple modification, a higher gain can be achieved when compared to the corresponding circuit implemented with resistors for the same DC voltage drop. Moreover, by proper biasing, it can be optimized to minimize the impact on circuit linearity (IIP_2 and IIP_3) without affecting the input impedance and the noise figure. The only limitation is the need of an extra reference voltage to to bias the CS stage. Simulation results with a 130 nm CMOS technology show that the gain of the proposed balun LNA is continuously tunable between 12 and 20 dB, and the NF is below 3.2 dB for a power consumption of 4.8 mW.

CHAPTER 5

LNAs WITH DOUBLE FEEDFORWARD AND WITH DOUBLE FEEDBACK

5.1 Introduction

In the previous chapter a LNA operating at 1.2 V with controllable gain was presented. In this chapter two solutions are proposed to boost the LNA gain without degrading the input matching constraint. Two techniques using local feedback are introduced, namely double feedforward (DFF) and double feedback (DFB). Two circuit prototypes in a 130 nm standard CMOS technology with 1.2 V and 0.6 V supply have been designed and simulated to demonstrate the proposed techniques.

5.2 LNA with Double FeedForward

As it has been demonstrated in the previous chapter, the traditional CS-CG LNA with resistors replaced by active loads has the advantage of achieving a higher gain, when compared to the same circuit with resistive loads under the same bias current. The active loads provide an additional degree of freedom in the LNA design, since the loads resistance can be changed through the biasing of PMOS

transistors. By using their gates to inject the RF signal, a loop is formed and the PMOS transconductance can be used to enhance the gain.

In Fig. 5.1, the proposed LNA circuit using a double feedforward structure is shown. Since the transconductance of M_1 is set by the 50 Ω input matching,

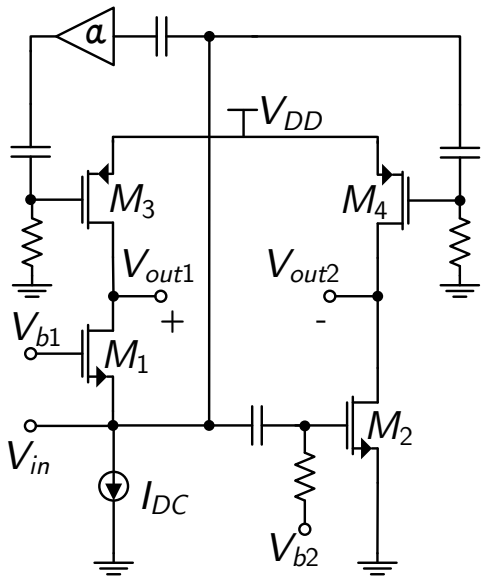


Figure 5.1: LNA with double feedforward.

this stage can only be boosted by acting upon the load. In the CG stage, the input signal is applied to a feedforward loop using an inverter gain block with gain α variable between -1 and -4. This inversion is required, since the CG stage does not change the signal phase. The resulting signal from the inverter gain block is inverted again when applied to M_3 transistor's gate and added to the output.

In the CS stage, the feedforward is straightforward, since the input signal is inverted when applied to the gate of M_4 (the circuit can be seen as common-source stage). As for the transconductance of M_2, it can be set without any limiting constraint, as long as the CS stage gain is the same as the CG: a simple coupling with unity gain can be used. Simulations have shown that there is no advantage in adding a gain block in this loop. The input signal is then amplified by the two common-source stages and the outputs are in phase opposition. The overall gain is boosted by the combination of active loads and feedforward.

To derive the equation for the gain, the circuit with active loads without the

feedforward loops is considered first:

$$A_v = g_{m1}(r_{o1}//r_{o3}) + g_{m2}(r_{o2}//r_{o4}) \tag{5.1}$$

Then, for the circuit of Fig. 5.1, it must be added to equation (5.1) the gain boost factor of the double feedforward, as follows:

$$A_v = (g_{m1} + |\alpha| g_{m3})(r_{o1}//r_{o3}) + (g_{m2} + g_{m4})(r_{o2}//r_{04}) \tag{5.2}$$

where g_{mi} and r_{oi} represent the transistors transconductance and drain-to-source resistance, respectively.

Regarding the noise, with this feedforward structure there is the additional noise of the inverter amplifier in the loop, but it can be minimized by proper design.

5.3 LNA with Double Feedback

As pointed out previously, the active loads allow the use of the technique of gain boosting through local feedforward loops. However, it would be desirable to avoid the inverter amplifier. To obtain a high gain, while maintaining a low noise figure, alternatives are investigated using the same principle of gain boosting and noise cancellation, but with focus on a circuit simplicity. With this goal in mind, a circuit with both local feedforward and feedback (FFB) is investigated, as shown in Fig. 5.2.

By taking the advantage of using transistors as active loads, V_{in} is applied to the gate of transistor M_4, is amplified and added to V_{out2}. The resulting signal is amplified through M_3 by feedback and added to V_{out1}. With this structure there is a significant increase in the gain, mainly in the CG stage, which needs to be carefully designed to ensure 50Ω input matching. In this case the thermal noise of M_1 is only partially cancelled, which degrades the LNA noise figure. To overcome this issue, a new circuit approach is proposed, in which a double feedback (DFB) structure is used, as shown in Fig. 5.3. In the DFB LNA (Fig. 5.3), V_{in} after amplification in the CG stage (M_1) is applied to the gate of M_4, in which it is further amplified and

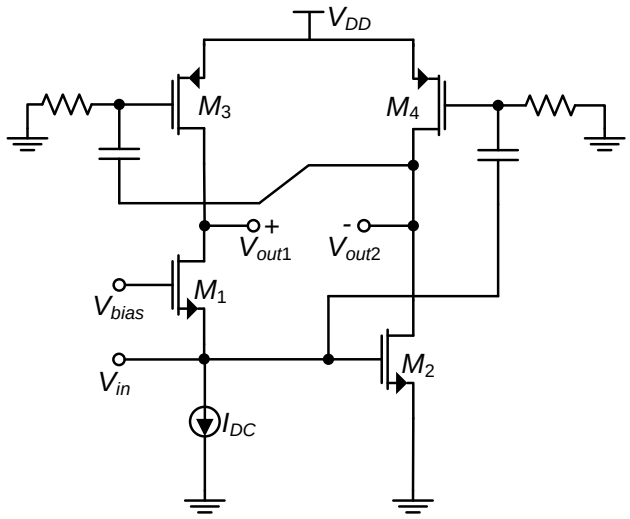


Figure 5.2: LNA with local feedforward and feedback.

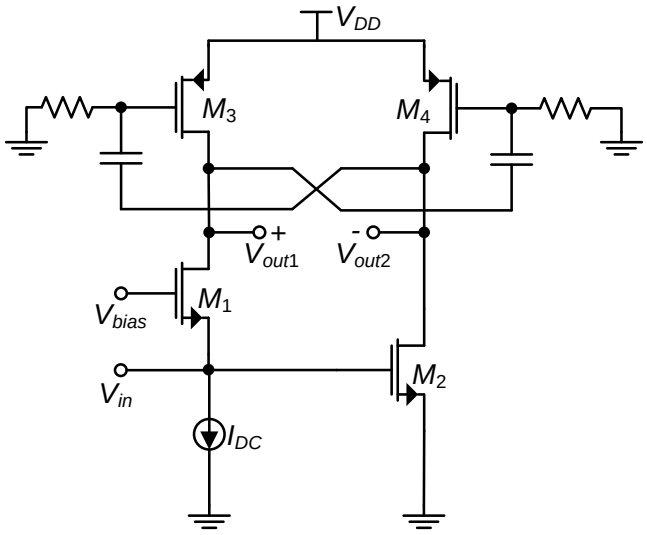


Figure 5.3: Proposed LNA using double feedback.

added to V_{out2}. The resulting signal is amplified trough M_3, and added to V_{out1}. With this structure there is a significant gain increase. The gain is boosted without using extra circuitry, and the noise of M_1 appears with the same level at the LNA outputs (load transistors M_3 and M_4), while the output signals remain balanced. This circuit is simpler and completely symmetrical, and therefore, it is expected to achieve better performance.

In the feedback a high pass RC coupling is used. With these connections, the parasitic capacitances of M_3 and M_4 (the gate-source and gate-drain capacitances)

will reduce the bandwidth , but the main goal is achieved: high gain and low NF.

The PMOS loads could be biased in saturation, which would lead to a higher gain due to the increase of the channel resistance. However, the circuit would have DC voltage instability, requiring a common-mode feedback (CMFB) type regulation circuit. Moreover, in the presence of mismatches, noise cancellation is still partially achieved, but distortion cancellation would be severely degraded [49].

In order to provide some circuit insight, the equations for the gain (CG and CS stages) and LNA input impedance are derived (for the proposed DFB circuit):

$$\frac{V_{out1}}{V_{in}} = \frac{g_{mCG}g_2 + g_{m2}g_{m3}}{g_1g_2 - g_{m3}g_{m4}} \tag{5.3}$$

$$\frac{V_{out2}}{V_{in}} = -\frac{g_{m2}g_1 + g_{mCG}g_{m4}}{g_1g_2 - g_{m3}g_{m4}} \tag{5.4}$$

where, $g_{mCG} = g_{m1} + g_{ds1}$, $g_1 = g_{ds1} + g_{ds3}$ and $g_2 = g_{ds2} + g_{ds4}$.

Using (5.3) and (5.4), the LNA differential gain is obtained,

$$A_{v,Diff} = \frac{V_{out1} - V_{out2}}{V_{in}} = \frac{g_{mCG}(g_{m4} + g_2) + g_{m2}(g_{m3} + g_1)}{g_1g_2 - g_{m3}g_{m4}} \tag{5.5}$$

The input impedance is,

$$Z_{in} = \frac{g_1g_2 - g_{m3}g_{m4}}{g_{mCG}(g_2g_{ds3} - g_{m3}g_{m4}) - g_{m2}g_{m3}g_{ds1}} \tag{5.6}$$

Using equations (5.5) and (5.6), the circuit performance can be optimized in order to increase the gain, minimizing the impact on the input matching.

From [8], [9], if it is assumed that $g_{m1} = g_{m2} = g_m$ and $r_{ds3} = r_{ds4} = r_{ds}$, the noise factor is:

$$F_{LNA} = 1 + \frac{k_f}{8kTR_Sc_{ox}f^{\alpha_f}}\left(\frac{1}{W_1L_1} + \frac{1}{W_2L_2} + \frac{1}{W_3L_3} + \frac{1}{W_4L_4}\right) + \frac{\gamma}{2R_Sg_m} + \frac{1}{R_Sr_{ds}g_m^2} \tag{5.7}$$

where k is Boltzmann's constant, c_{ox} is the oxide gate capacitance per unit area, W_i and L_i are the transistor dimensions, T is the absolute temperature, γ is the excess noise factor, k_f and α_f are intrinsic process parameters, which depend on the size

of the transistors [47], [48]. The main noise sources in this type of LNA are those of M_1 (the thermal noise is cancelled) and those of M_2, while the noise introduced by the loads is significantly lower.

From [8], to improve the noise figure, g_{m2} should be higher than g_{m1}, while g_{ds4} is increased to keep the output signals balanced:

$$g_{m2} = \alpha \cdot g_{m1}$$

$$g_{ds4} = \alpha \cdot g_{ds3}$$

The optimal value of α is obtained by simulation and it was found to be approximately 1.5.

5.4 Simulation results

5.4.1 LNA with Double FeedForward

One of the advantages os using gain boosting is that it allows to reduce the power consumption while achieving an acceptable gain. To prove the feasibility of the LNA with double feedforward with very low voltage supply and to evaluate its the performance, two circuit prototypes were designed using a 130 nm CMOS standard technology, one with 1.2 V supply voltage and the other with 0.6 V supply.

In the LNA prototype with 1.2 V supply, the transistors have $W_1 = 67.2$ µm, $W_2 = 115.2$ µm and $W_3 = W_4 = 12.4$ µm. For maximum speed, all transistors have the minimum channel length (120 nm). The current source that bias the CG stage is set to 2 mA and the gain block is an inverter based amplifier with resistive feedback self-bias.

For the LNA prototype with 0.6 V supply, the transistors widths are to $W_1 = 80$ µm, $W_2 = 92.8$ µm and $W_3 = 48$ µm and $W_4 = 57.64$ µm. All transistors have the minimum channel length. The current source that bias the CG stage is set to 1.35 mA, and the gain block is an inverter based amplifier using a Dynamic Threshold MOS (DTMOS) structure [50], in order to reduce the resistive noise contribution and also to better cope with the low voltage supply requirements.

Table 5.1: Circuit simulations for 1.2 and 0.6 supply voltage.

V_{DD} [V]	Circuit	BW [GHz]	A_v [dB]	NF [dB]	IIP3 [dBm]	P_{DC} [mW]	FOM $[mW^{-1}]$
1.2	$\alpha = -1$	0.1-7.4	20.3	< 3.2	-4.2	5.4	1.7
	$\alpha = -4$	0.1-5.9	21.9	<3	-8.6	6.2	2.0
0.6	$\alpha = -1$	0.1-3.4	21.1	<3	-16.7	2.1	5.4
	$\alpha = -4$	0.1-1.3	23.9	<3.2	-26	2.25	6.4

In order to investigate the influence of feedforward on the circuit key parameters, gain, bandwidth, noise figure, and linearity, several simulation results are presented in table 5.1. Four cases are considered for the double feedforward LNA: using a gain of -1 or -4 for the inverter amplifier with 1.2 V and 0.6 V supply voltage. For comparison the following figure of merit is used [51]:

$$FOM[mW^{-1}] = \frac{Gain}{(F-1)P_{DC}[mW]} \tag{5.8}$$

From Table 5.1, it is seen that with 1.2 V, there is a significant increase of the gain, without penalty in the NF. This is also shown in Figs. 5.4 and 5.5. The disadvantages are the increase of circuit non-linearity and a reduction of the available bandwidth. The FOM is similar for both cases.

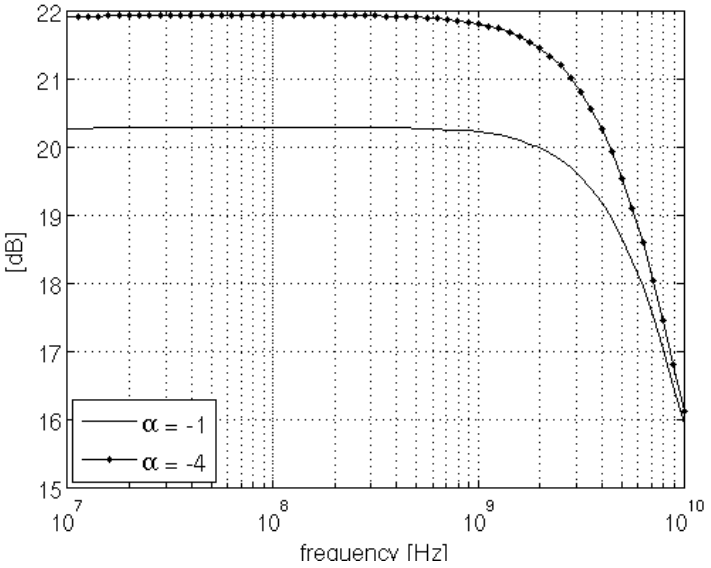


Figure 5.4: Gain simulations for the circuit with 1.2 V supply.

The circuit prototype operating at 0.6 V has similar performance in terms of gain and NF, when compared with the circuit operating at 1.2 V, as shown in Figs.

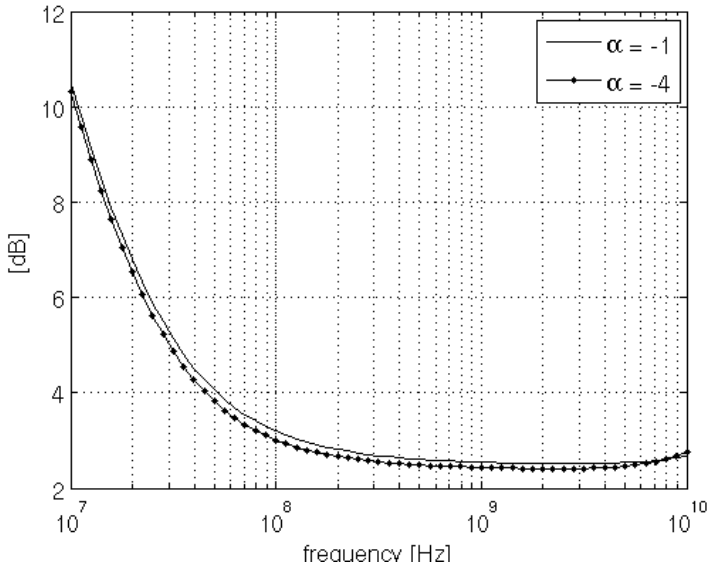


Figure 5.5: NF simulations for the circuit with 1.2 V supply.

5.6 and 5.7, but there is a strong reduction of power consumption, which leads to the best FOM.

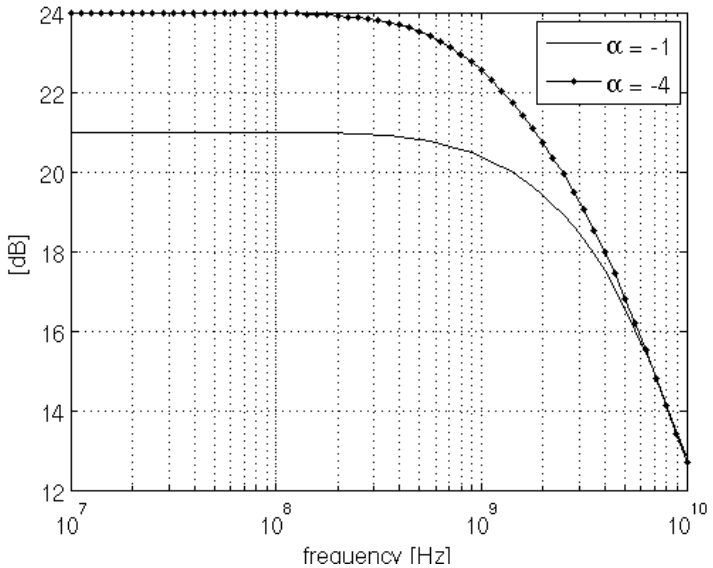


Figure 5.6: Gain simulations for the circuit with 0.6 V supply.

When comparing the simulation results with those in the literature, the circuit operating at 0.6 V is very good in terms of gain and NF, and has very low power. The proposed approach is especially interesting in low power and low voltage biomedical applications [3]. Since in these applications low power is essential, but

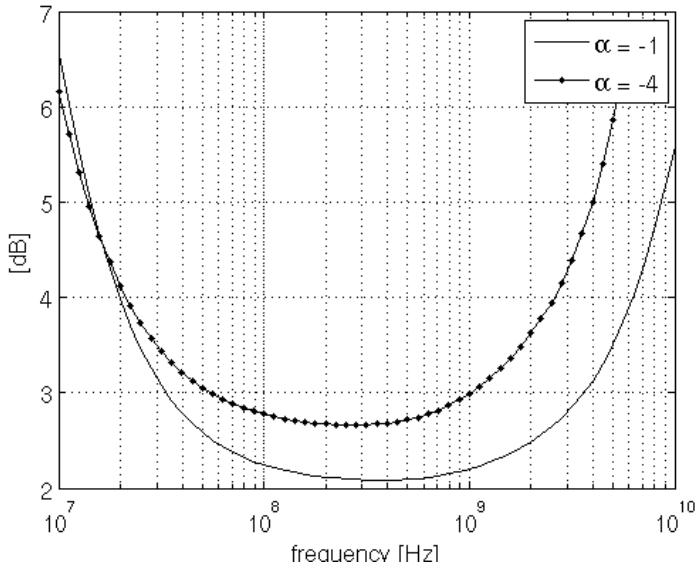


Figure 5.7: NF simulations for the circuit with 0.6 V supply.

some non-linearity can be tolerated, usually, the target application only needs a low data rate communication link. There are ISM bands in 450 MHz and 900 MHz and a WMTS band in 600 MHz, for which this circuit can be a good alternative to the conventional solutions.

5.4.2 LNA with Double Feedback

The proposed circuit was designed using Cadence Spectre RF simulator (SP, PSS, PNOISE), using BSIM v3.3 models from standard CMOS 130 nm technology with 1.2 V supply. The circuit parameters are given in Table 5.2. The transistors have minimum length to maximize speed, and V_{bias} is 795 mV.

Table 5.2: LNA circuit parameters using DFB.

	I_D [mA]	W [µm]	r_{ds} [Ω]	g_{ds} [mS]	g_m [mS]
M_1	2	139.2	420	2.38	30.7
M_2	2.4	358.4	355	2.82	44.4
M_3	2	13.1	236	4.24	2.1
M_4	2.4	16.2	187	5.35	2.5

To compare the proposed architecture with the others mentioned above, the theoretical and simulated results for the optimized voltage gain are compared, as

shown in Table 5.3. Regarding the theoretical results, equation (4.2) is used for the LNA of Fig. 3.1 with resistors [8] and for the circuit using active loads with MOS transistors biased in triode (Fig. 4.1), where the values of R_1 and R_2 are used instead of g_{ds3} and g_{ds4}, respectively, for the case with resistors. Equation (5.2) is used for the DFF LNA (Fig. 5.1), and equation (5.5) for the proposed DFB circuit.

Table 5.3: Optimized voltage gain (dB) for different topologies.

Load	Resistor [Fig. 3.1]	MOS [Fig. 4.1]	DFF [Fig. 5.1]	DFB [Fig. 5.3]
Theoretical	18.4	19.9	22.2	23.3
Simulation	18.1	19.7	21.9	23.9

In order to investigate the influence of DFB on the LNA key parameters: gain, noise figure, linearity, and frequency band, several simulation results are presented in Table 5.4. The circuits were designed for gain optimization and under the same conditions, with ideal biasing circuitry and with an ideal current source of 2 mA, to highlight the advantages and trade-off of each circuit. For a convenient comparison of the results obtained, the figure of merit in (5.8) is used [51]:

Table 5.4: Circuit simulations for different topologies with 1.2V supply.

Load	**Resistor** [Fig. 3.1]	**MOS** [Fig. 4.1]	**DFF** [Fig. 5.1]	**DFB** [Fig. 5.3]
Gain [dB]	18.1	19.7	21.9	23.9
NF [dB]	<3.1	<2.9	<3	<1.8
IIP3 [dBm]	8.2	-3.4	-8.7	-13.1
Power [mW]	5.2	4.9	6.3	5.3
Band [GHz]	0.1-10	0.1-5.8	0.1-5.8	0.1-2.2
FOM1 [mW^{-1}]	1.48	2.07	1.98	5.76

The results in Table 5.4 show that the DFB leads to the highest gain and the lowest NF, leading to the highest FOM. The disadvantages are the increase of the circuit non-linearity and the reduction of the bandwidth.

In Figs. 5.8 to 5.10, the simulation results for the input match (S_{11}), gain, and NF, for the proposed circuit (DFB) are presented, leading to the best FoM, since with the proposed DFB circuit the highest gain and lower NF are obtained.

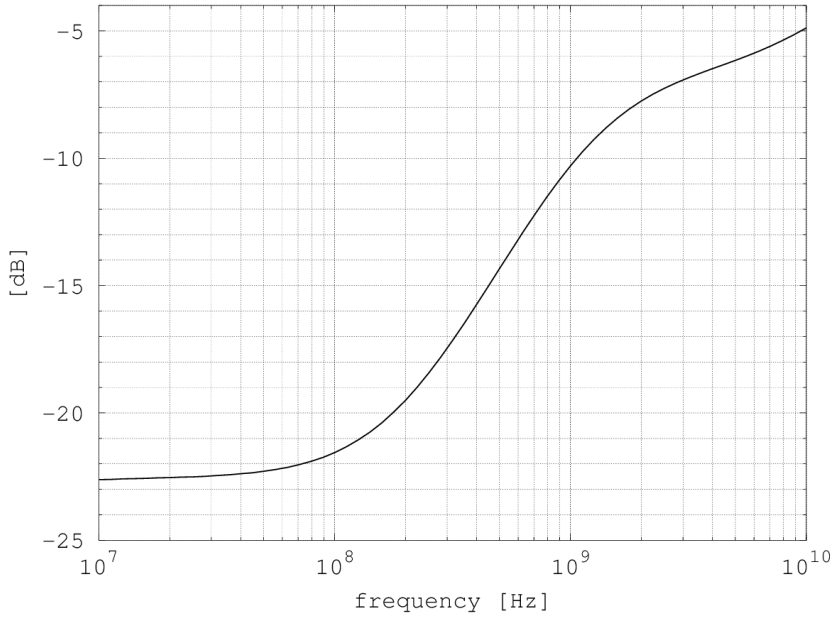


Figure 5.8: Simulated S_{11} parameter for the DFB LNA.

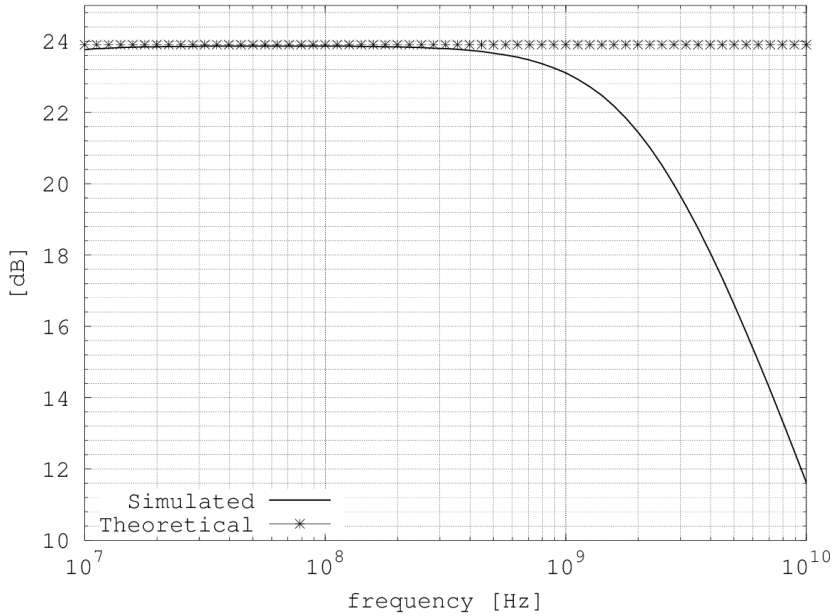


Figure 5.9: Simulated gain for the DFB LNA.

5.5 Discussion and conclusions

In this chapter, two LNA circuit approaches are presented, a wideband balun LNA with double feedforward and other using a double feedback. In the case of the DFF LNA, two circuit prototypes operating at 1.2 V and 0.6 V were designed to validate the proposed methodology. A circuit using DFB was also designed for high gain

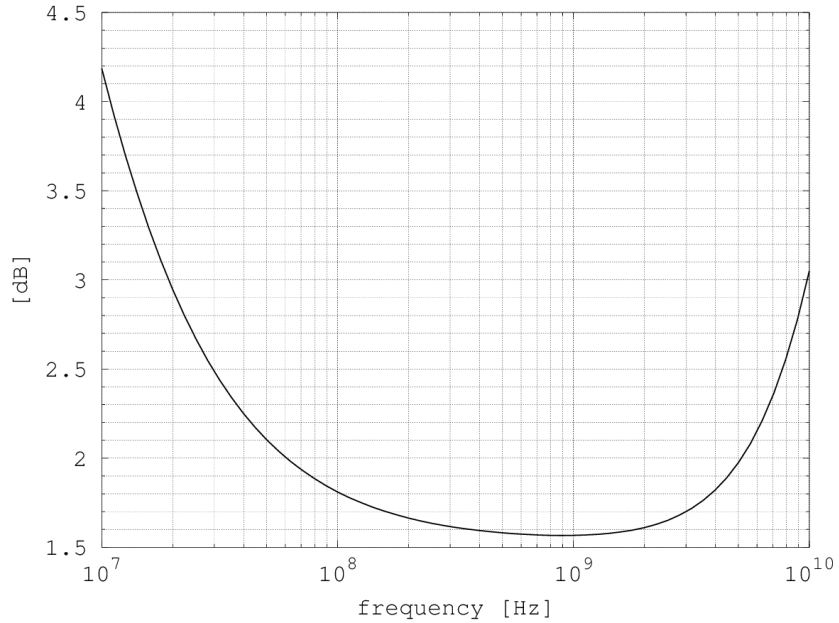


Figure 5.10: Simulated NF for the DFB LNA.

and low NF operating at 1.2 V. Simulation results have shown that this last circuit presents the best performance when compared to the conventional CG-CS LNA implemented with resistors and with the other circuits proposed in this thesis. The simulated gain of the balun DFB LNA is 23.8 dB, and the NF is below 1.8 dB, for a power consumption of 5.3 mW. The proposed circuits are especially useful for low power and low voltage operation in biomedical applications (ISM and WMTS bands).

CHAPTER 6

MEASUREMENT RESULTS

6.1 Introduction

This chapter is devoted to the experimental results and measurements set up of the implemented prototypes. To validate the proposed circuits and techniques described in this thesis, two prototypes were designed using the CMOS 130 nm technology from UMC. The first prototype is an LNA with active loads, the performance of which is compared with that of an LNA implemented with resistors using the same measurement setup. The second prototype is an RF front-end block, using the double feedback LNA proposed in chapter 5 to prove its functionality from a system perspective. For comparison purposes, another version of the RF front-end was also implemented, using the LNA with active loads from the first prototype.

6.2 LNAs with resistive and with active loads

In order to demonstrate the potential of the LNA using active loads, two prototypes were designed and implemented, the one represented in Fig. 4.1 and its resistive version (Fig. 3.1), and their overall performance is compared.

As already stated, the value of g_{m1} is set by the required input impedance (50 Ω) (approximately $1/g_{m1}$). The transconductance of M_2 should be equal to that of M_1, which, with equal loads, leads to equal gains as required for gain matching and noise cancellation.

The transistor widths are set to $W_1 = 80$ μm, $W_2 = 89.6$ μm and $W_3 = W_4 = 12.3$ μm (values obtained from post-layout simulations including the biasing and buffer circuits). For maximum speed, all transistors have the minimum channel length (120 nm). The bias voltage $V_{bias} = 930$ mV sets the value of V_{GS2}, since V_{GS1} is defined by the current source I_{DC}.

For a fair comparison, equal voltage drops are considered in the load devices in the two cases, and the load resistances have a value of about 200 Ω, similar to the work in [8], and the transistors as active loads have $g_{ds} = 3.9$ mS, which was obtained using the maximum gain point as shown in Fig. 4.2. The active loads are not in saturation, and the equivalent resistance is increased from 200 to 256 Ω.

For each case, results from schematic and post-layout simulation, and measurements are presented for comparison. Both circuit prototypes use the same test setup biasing circuitry and an internal balun/output buffer, as shown in Fig. 6.1, and they have been built together in the same multi-project wafer (MPW) run.

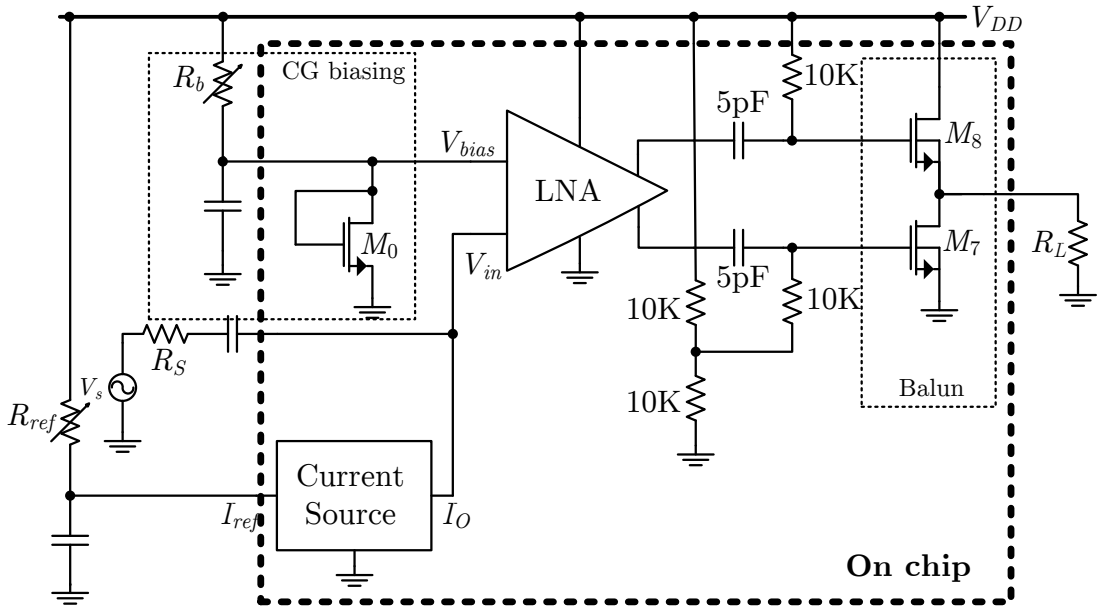


Figure 6.1: LNA test setup for evaluation of the integrated prototypes.

In Fig. 6.2 the layout and die photo of the two circuits are shown. The area of each chip is 198 x 390 µm (including pads), and the two chips have approximately the same area, since there is a negligible difference between the areas of the load transistor and of the load resistor.

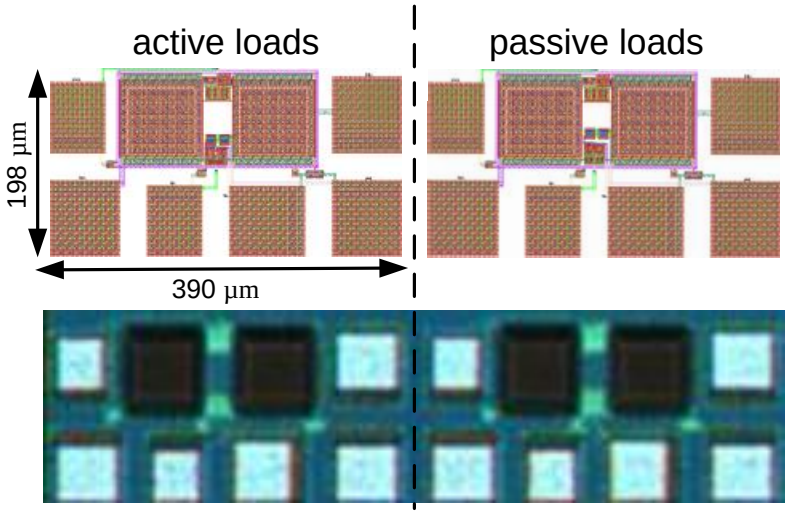


Figure 6.2: Layout and die photo of the LNAs with active and passive loads.

The bias current source is implemented employing a simple current mirror, and a biasing circuitry is used for biasing the gate terminal of transistor M_1 (Fig. 6.1). At the output an internal balun / voltage-combiner [52] is used for differential to single-ended conversion and for matching the 50 Ω standard impedance of the measuring equipment. This allows testing with the LNA directly connected to the network and spectrum analyser for measuring the S-parameters, Gain, NF, and IIP3.

A photo of the test board is shown in Fig. 6.3. The chip is connected to the board by direct wirebonding, and microstrips and RF coaxial sub-miniature version A (SMA) conectors are used for testing the LNAs.

In Figs. 6.4, 6.5, 6.6, and 6.7 are presented the results of gain and NF for the two LNAs. The fluctuations in the curves are due to the external interference captured by the test boards, due to a strong WiFi signal at 2.4 GHz, which are not related with the integrated circuit prototype.

In Table 6.1 a comparison is presented between the traditional version with passive loads and the proposed version with active loads. To compare the two

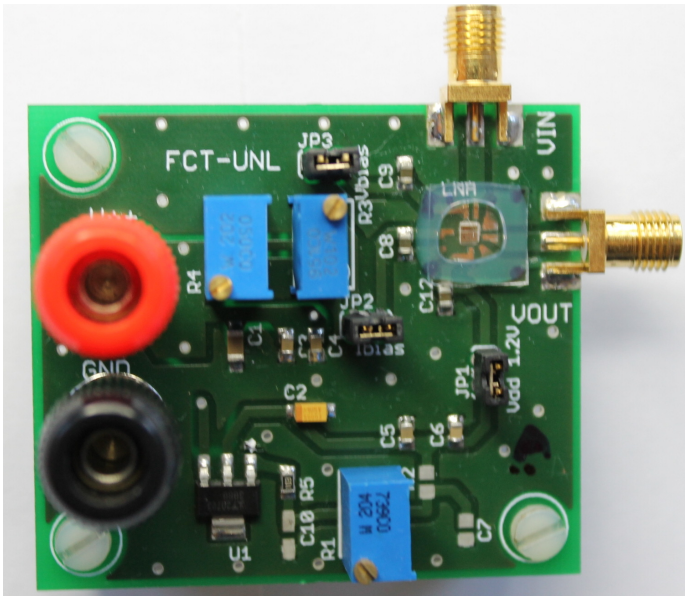


Figure 6.3: LNA test board.

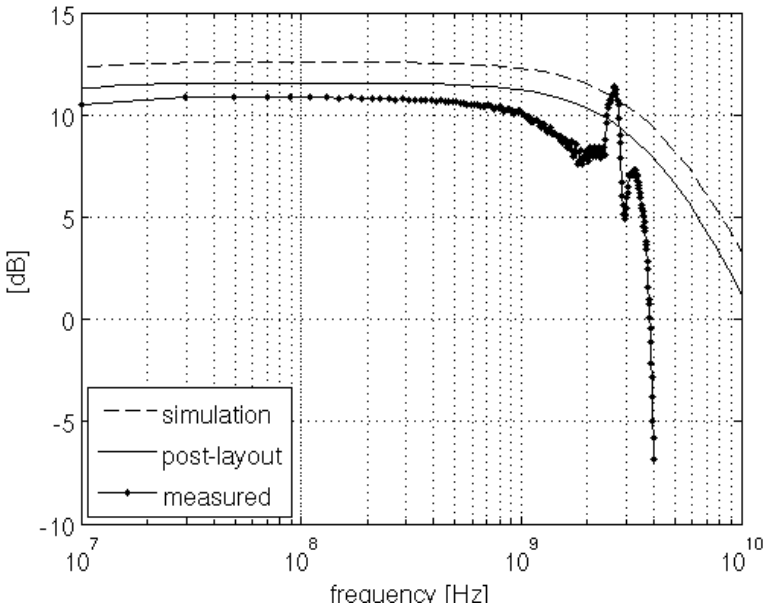


Figure 6.4: Power gain of the LNA with active loads.

cases, the FoM defined in (2.25) is used. This circuit is suitable, in the region up to 1.5 GHz, for ISM bands (450 MHz, 900 MHz), and WMTS band (600 MHz and 1.4 GHz) [3]. An example at 600 MHz is considered, and similar results are obtained for the remaining bands as shown in Figs. 6.8 and 6.9.

The proposed LNA has lower power consumption (4.8 mW) than the LNA in [8] (14 mW), in which the bias current of the CS stage is four times that in the

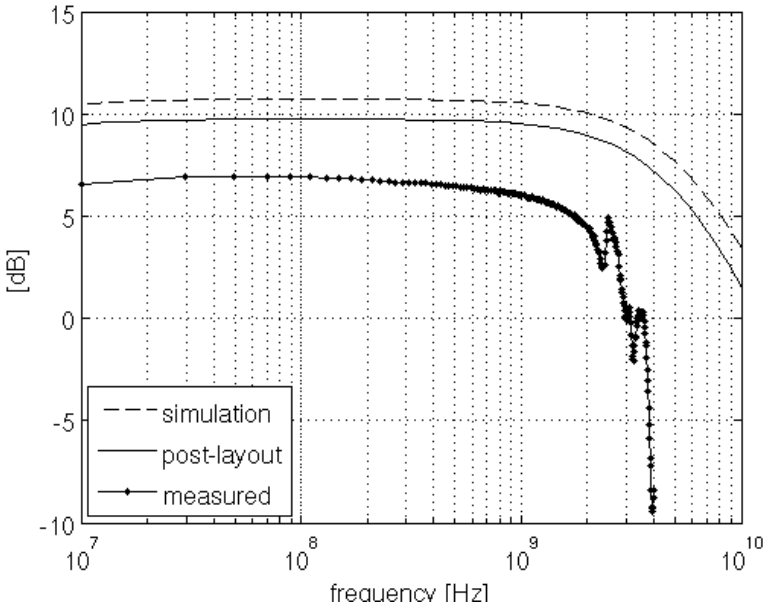


Figure 6.5: Power gain of the LNA with passive loads.

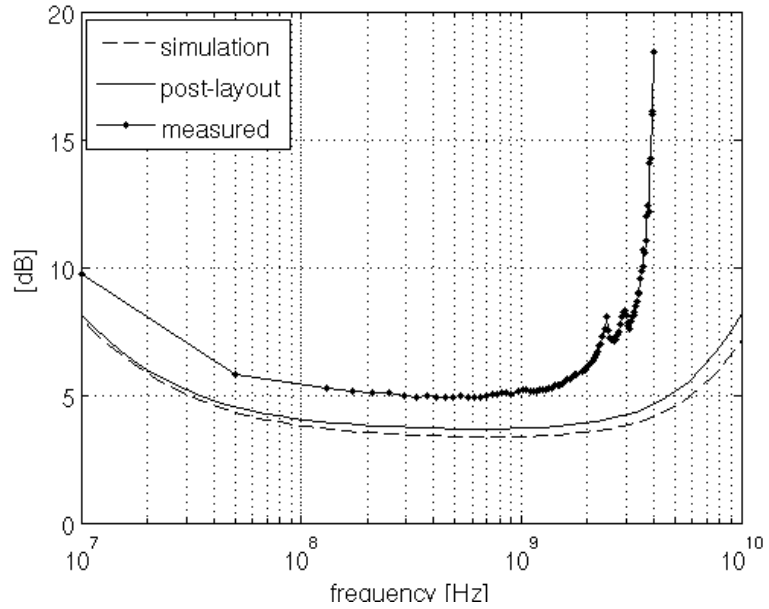


Figure 6.6: NF of the LNA with active loads.

CG stage. Here, the current source I_{DC} is implemented within the chip, which is responsible for about 1 dB degradation in the NF, whereas the authors of [8], have used an inductor connected in series with the source of the CG stage. In order to simplify the measurements, in the test circuit a balun/buffer is included, which leads an increase of only 0.3 dB in the LNA NF. To confirm this, a noise simulation

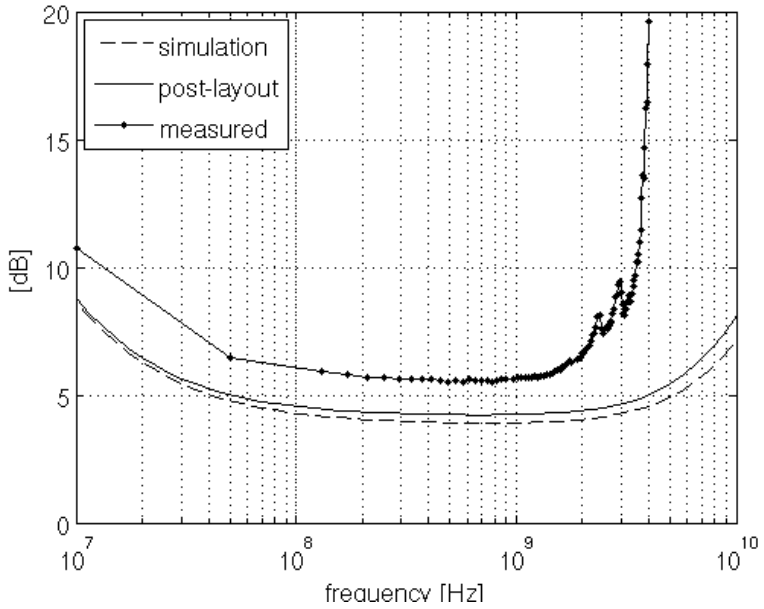


Figure 6.7: NF of the LNA with passive loads.

Table 6.1: Circuit measurements for active and passive loads considering WMTS biomedical application [3]

Loads	**Freq. [GHz]**	**Power gain [dB]**	**NF [dB]**	**IIP3 [dBm]**	**P_{DC} [mW]**	**FOM $[mW^{-1}]$**
Passive loads	0.6	7	5.4	-3.8	4.8	0.4
Active loads	0.6	10.8	4.9	1.5	4.8	0.7

was performed in which the noise summary was listed for the 10 dominant noise sources, at 600 MHz, and the contribution of the gate noise current and of the biasing circuit of the CG stage are negligible (below 1 % of the total output noise).

Measuring the LNAs with a double-layer PCB board using wirebonding, two micro-strips, and two SMA connectors, and with a DC block at the LNA input, leads two more than 1 dB NF degradation with respect to post-layout simulations for both circuit prototypes. This NF degradation with respect to the post-layout simulations could be strongly reduced by using a probe station with on-wafer testing, but this is not available in the lab where the measurements were performed. These cumulative NF degradation explains the differences between the NF measured in [8] and the results obtained in Table 6.1.

From Table 6.1 and Figs. 6.8 and 6.9, it can be observed that the proposed circuit

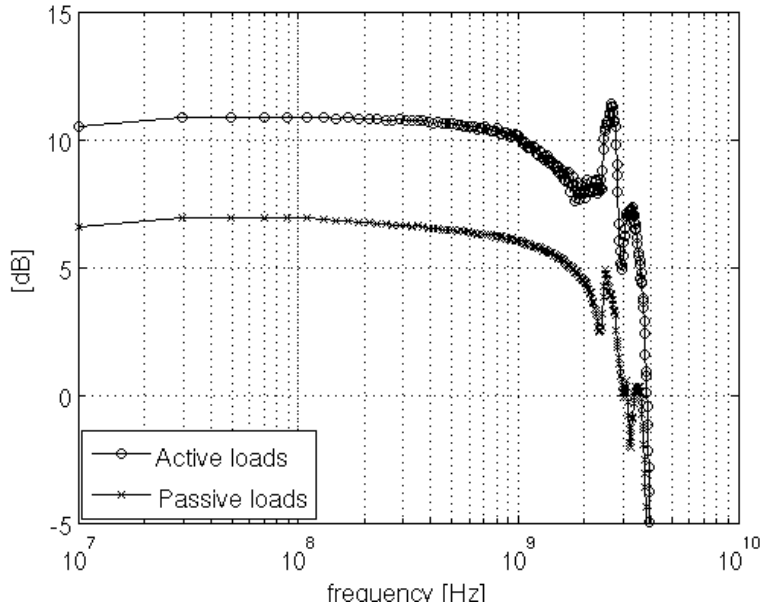


Figure 6.8: Comparison of measured LNA gain with active and passive loads.

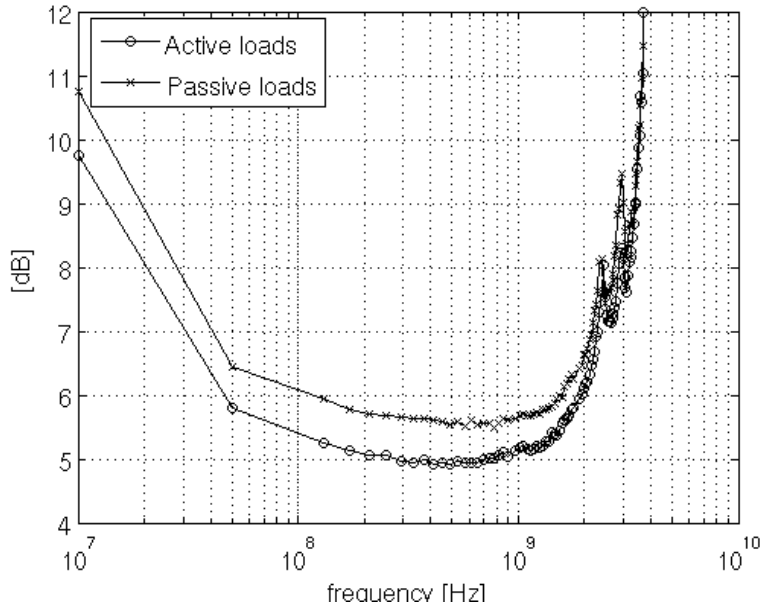


Figure 6.9: Comparison of measured LNA NF with active and passive loads.

has a higher measured gain (up to 3 dB improvement) and lower NF (about 0.5 dB reduction), with a similar performance in terms of non-linearity. The improvement in NF is due to the increased gain, since the noise contributions of the resistor and of the transistor loads are similar.

In Table 6.2, the performance of this circuit is compared with some state-of-the

Table 6.2: Comparison with state-of-the-art LNAs.

Ref.	**Tech. [nm]**	**BW [GHz]**	**A_v [dB]**	**NF [dB]**	**IIP3 [dBm]**	**P_{DC} [mW]**	**FOM $[mW^{-1}]$**
[8]	65	0.2-5.2	13-15.6	<3.5	>0	14	0.4
[53]	90	0.5-8.2	22-25	<2.6	>-16	42	0.5
[54]	90	0.8-6	18-20	<3.5	-	12.5	0.6
[55] [s]	90	0.1-1.9	20.6	<2.7	10.8	9.6	1.3
[56] [s]	130	0.2-3.8	11.2	<2.9	-2.7	1.9	2.1
[57]	180	0.5-0.9	16	<4.3	>-1.5	22	0.2
[58]	180	0.1-0.9	15	<4.2	2.6	10	0.3
This work	130	0.1-2	16.8	<5	1.5	4.8	0.7

[s] Simulation results

art wideband LNAs.

An LNA with passive resonating load might have a lower NF. The circuit prototype proposed here is a low area, low cost wideband LNA, and can be built in a standard CMOS technology. Since it is wideband, a steeper band selection filter may be required. The performance is worse than that of a resonating load LNA, but the circuit is wideband and can cover all the ISM and WMTS bands, from 450 MHz to 1.5 GHz. A passive resonating load circuit only works for a single frequency band; dual-band or multi-band approaches, which would have a large overhead in area and cost.

6.3 LNA with Double Feedback

Since the objective of the improved DFB LNA proposed in chapter 5 is to be applied in a low area and low power receiver, and to demonstrate that this objective can be obtained, it has been designed a RF receiver front-end, which is a modern discrete-time down-converter [18], [59] for ISM and WMTS bands with the block diagram represented in Fig. 6.10.

Two RF receiver front-end circuits were designed and fabricated in the UMC CMOS 130nm technology. For comparison purposes two versions of the receiver were implemented, one with the DFB LNA (receiver B), and the other with the basic LNA circuit of Fig. 4.1 using active loads (receiver A). All the remaining

blocks are the same in the two front-ends.

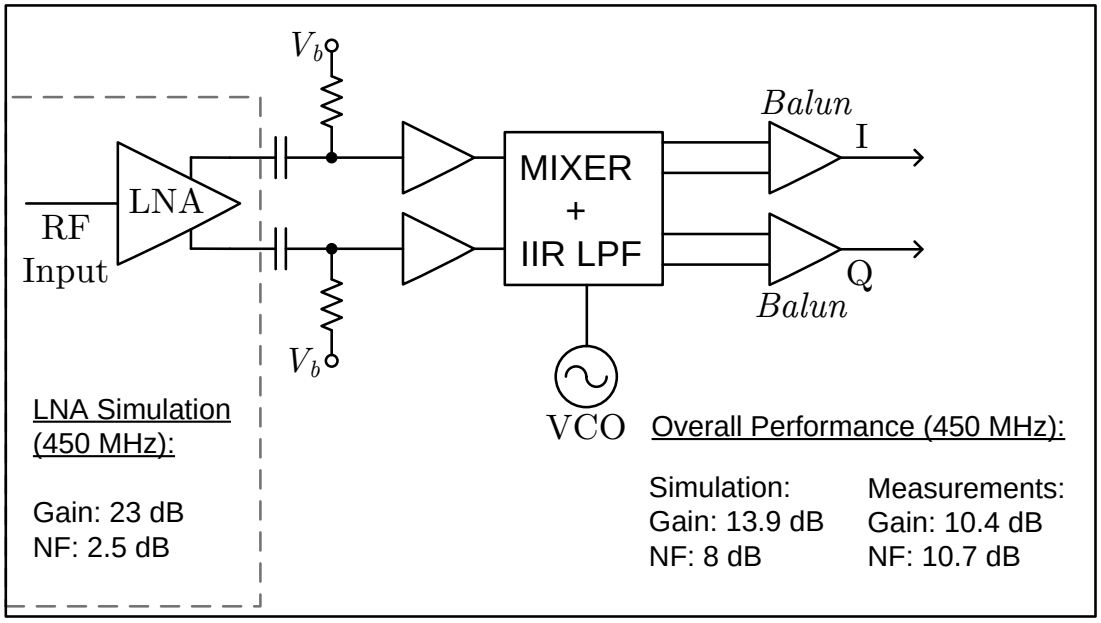
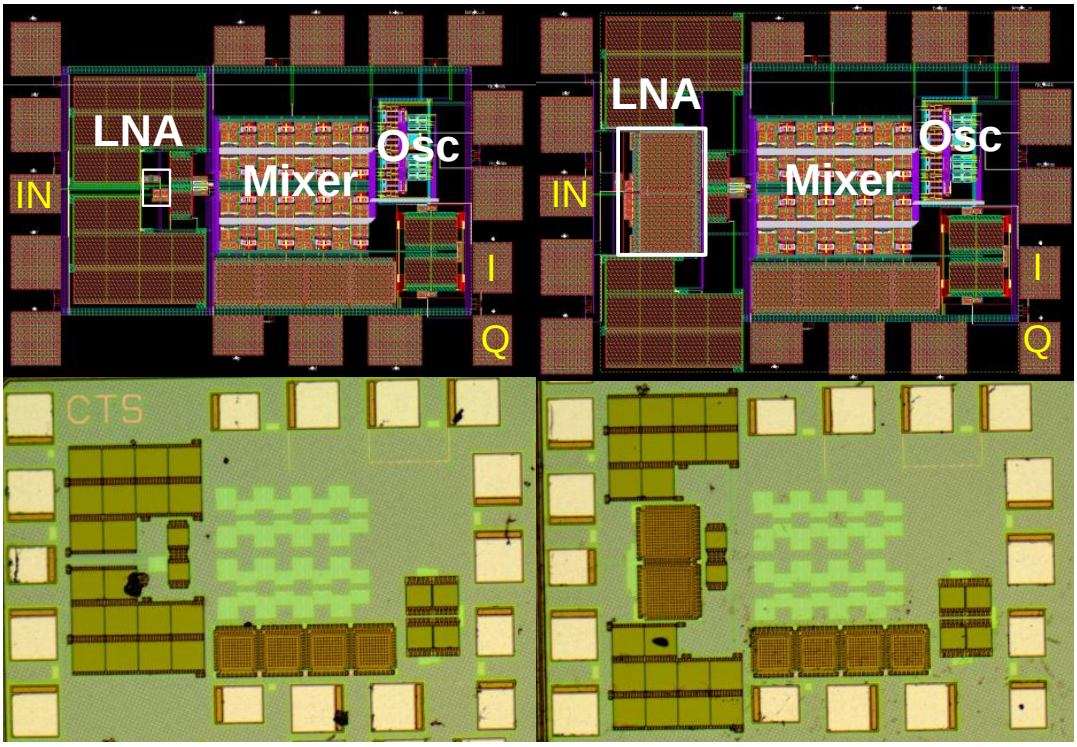


Figure 6.10: Block diagram of the implemented RF receiver front-end.

The overall area of each front-end is about 800x550 μm^2. The layout and die photo are shown in Fig. 6.11, where the main blocks and signal pads are highlighted. It is worth mentioning that although the DFB LNA has more area due to the cross-coupled capacitors, this does not affect the front-end overall area. The remaining pads are for supply and voltage references as well for external biasing circuits.

All the measurements were done with a spectrum analyser with a software option for noise figure measurements and a network analyzer for input matching verification (s_{11}). The test board developed for the measurements is shown in Fig. 6.12. The circuits were measured with an RF signal ranging from 250 to 900 MHz, which was limited by the internal voltage controlled oscillator (VCO) in terms of frequency.

The LNAs performance can be inferred from the measurement results, but the bandwidth can be estimated through the 1-port measurement of s_{11} as shown in Fig. 6.16. For each measurement step, the internal VCO has to be tuned to convert the RF signal to a low IF of 10 MHz. This tuning is performed by adjusting an external trimmer.



(a) (b)

Figure 6.11: Die photo and layout: (a) front-end with the LNA with active loads; (b) front-end with DFB LNA.

It was not possible to measure the LNA standalone performance, and therefore, the LNA results have to be extrapolated, by assuming that the difference from simulation and measurements is due to the LNA. This is a worst case assumption that guaranties that the actual performance cannot be worse than the extrapolated result.

In order to have the most accurate results of the LNA prototype, a post layout simulation of the LNA with the biasing circuitry included was performed, which has led to some degradation in the noise figure, mainly due to the current source. In this case the internal balun was not included in the simulations, since the LNA differential output can attack directly the filter preceding the mixer.

In Figs. 6.13 to 6.15, the simulation results for the input matching (s_{11}), gain, and NF, for the proposed DFB circuit prototype are presented.

From the measurements of the prototype with the proposed DFB LNA circuit there is a gain loss of 3.5 dB with respect to simulation, which it is assumed that

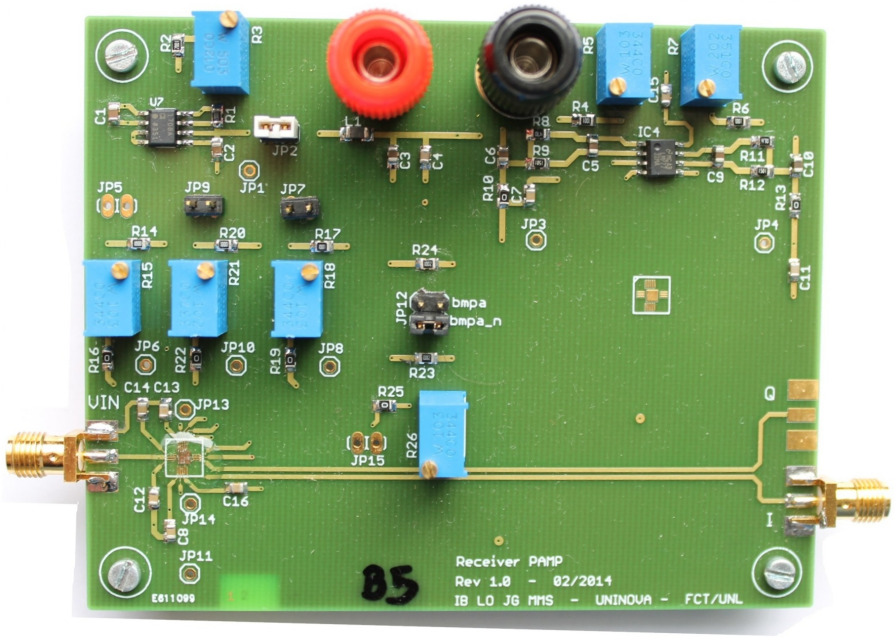


Figure 6.12: RF front-end test board.

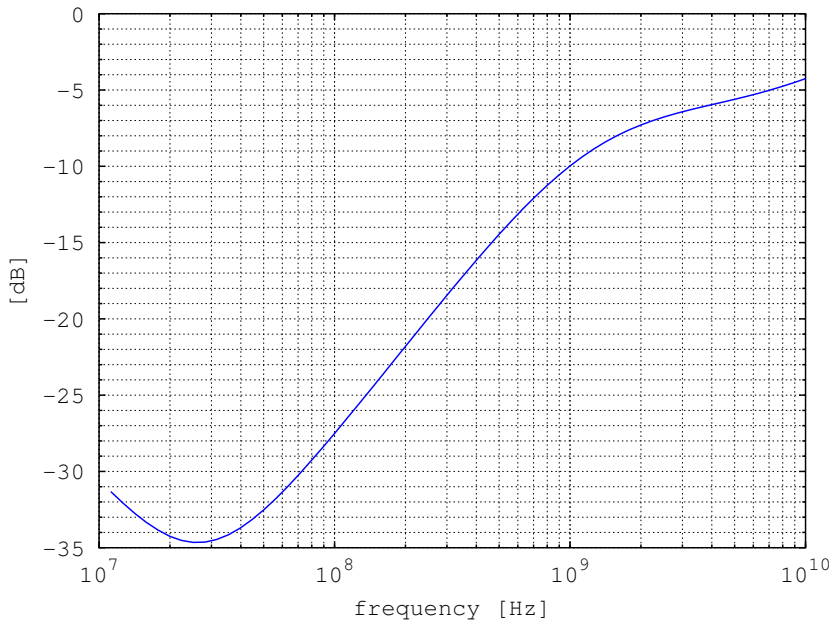


Figure 6.13: Post-layout simulation of S11 parameter for the DFB LNA.

was only due to the LNA. Thus, the LNA gain is higher than 19.5 dB. As for the NF, it has a degradation of 2.7 dB, which is also attributed to the LNA, since the overall NF is dominated by the first stage, and therefore, it can be assumed that the LNA NF is lower than 5 dB. Regarding IIP3, and considering the cascaded stages of the RF front-end, it is dominated by the second stage (i.e., mixer), and

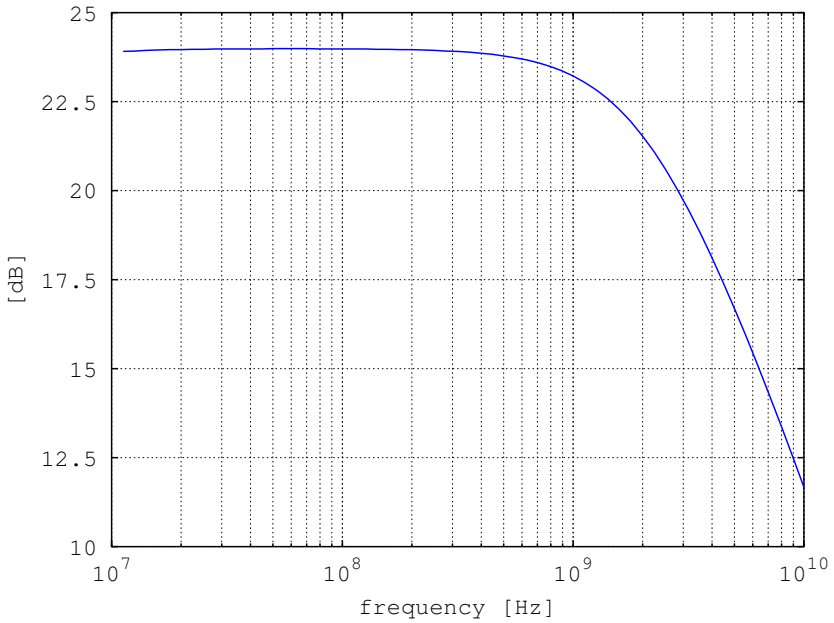


Figure 6.14: Post-layout simulation of gain for the DFB LNA.

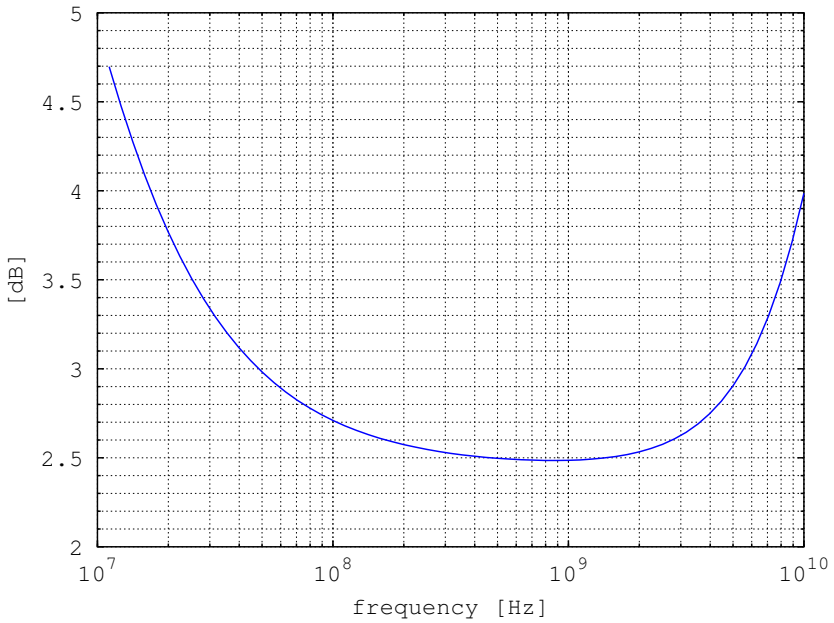


Figure 6.15: Post-layout simulation of NF for the DFB LNA.

therefore a IIP3 above 0 dBm is estimated for the LNA.

Comparing the two receiver designs, it is observed that the gain increases and the NF decreases for receiver B with the proposed DFB LNA, as shown in Figs. 6.17 and 6.18. The results in terms of linearity are similar, the IIP3 of receiver A is -4.9 dBm at 450 MHz, and the IP3 of receiver B is 0.3 dBm. However, for biomedical

applications the linearity is not a major concern.

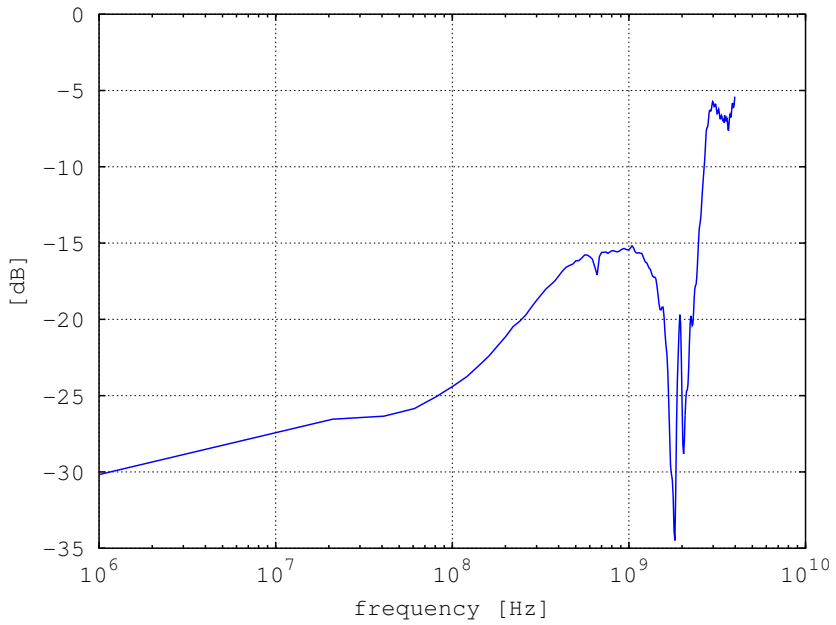


Figure 6.16: Measured s_{11} of DFB LNA (receiver B).

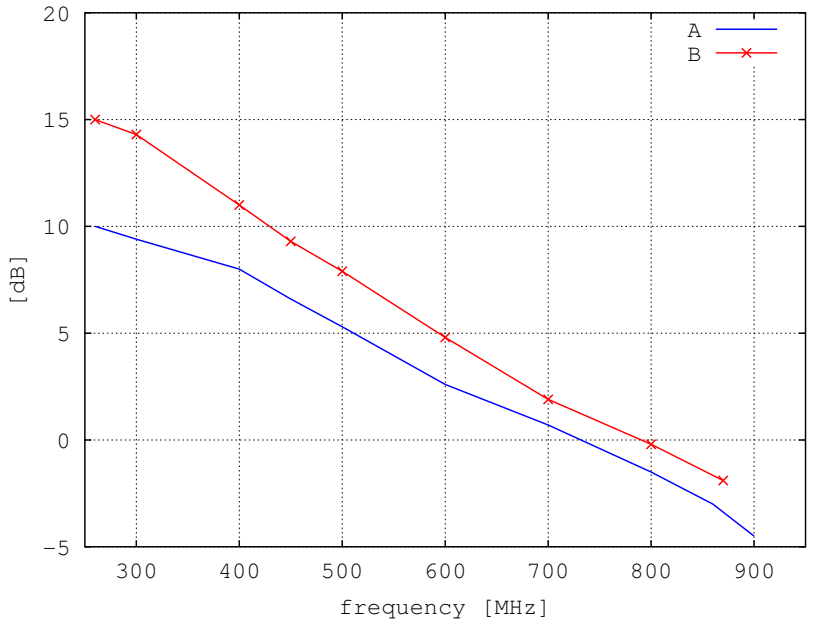


Figure 6.17: Measured front-end gain (receiver A and B).

Comparing these results with state-of-the art inductorless LNAs (Table 6.3), the post-layout simulations show that the proposed DFB LNA is very good in terms of gain and NF, and has very low power, which leads to the best FOM1. However, in order to have a fair comparison, the extrapolated results for the DFB LNA from

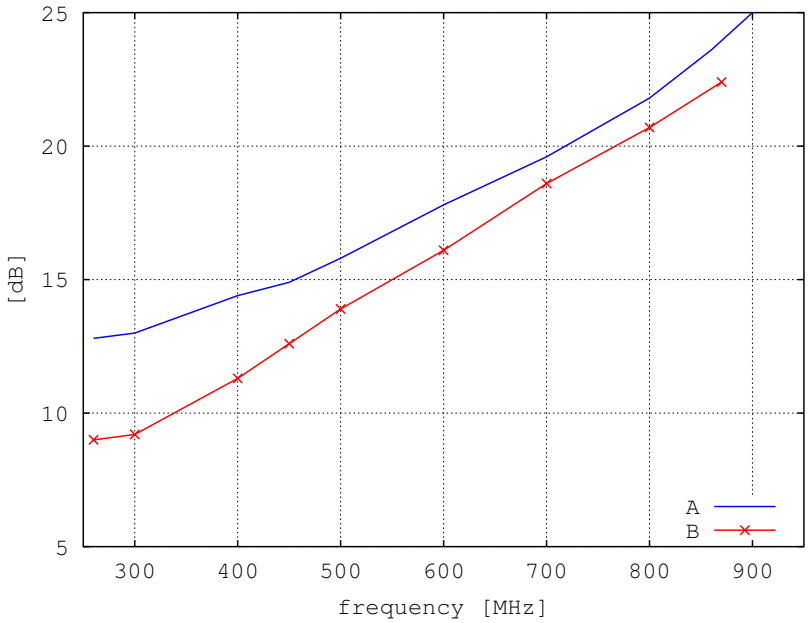


Figure 6.18: Measured front-end NF (receivers A and B).

the measured data of the RF front-end are also presented, in which all the losses are attributed to the LNA to assure that the real results are in fact better than the extrapolated ones. Since the LNAs have many performance parameters, a second

Table 6.3: Comparison with state-of-the art LNAs.

Ref	Techn. [nm]	Band [GHz]	Voltage Gain [dB]	NF [dB]	IIP3 [dBm]	Power [mW]	FOM1 [mW^{-1}]	FOM2 [-]
[8][m]	65	0.2-5.2	13-15.6	<3.5	>0	14	0.35	3.45
[53][m]	90	0.5-8.2	22-25	<2.6	-4/-16	42	0.52	0.13
[54][m]	90	0.8-6	18-20	<3.5	>-3.5	12.5	0.65	2.86
[55][s]	90	0.1-1.9	20.6	<2.7	10.8	9.6	1.29	154
[56][s]	130	0.2-3.8	11.2	<2.8	-2.7	1.9	2.11	11.2
[57][m]	180	0.5-0.9	16	<4.3	-	22	0.17	n.a.
[58][m]	180	0.1-0.9	15	<4.2	-	10	0.34	n.a
[9][m,a]	130	0.1-2	16.8	<5	>0	4.8	0.67	6.6
This Work[s]	**130**	**0.1-2.2**	**21-24**	**2.5-2.7**	**-7.6**	**5.4**	**3.4**	5.9
This Work[e]	**130**	**0.1-2.5**	**19.5**	**<5**	**>0**	**5.4**	**0.81**	8

[a] LNA with active loads
[e] Extrapolated results from measurements at 450 MHz
[m] Measurement results
[s] Simulation results

FOM (6.1) is also included in Table 6.3 that considers IIP3 and bandwidth [36].

$$FOM_2[-] = \frac{Gain \cdot IIP3[mW] \cdot f_c[GHz]}{(F-1) \cdot P_{DC}[mW]} \tag{6.1}$$

This FOM was originally used for narrowband LNAs, since the frequency of operation is considered instead of the bandwidth, which it is replaced here for a proper comparison of wideband LNAs. The proposed circuit approach using DFB is especially interesting in low power and low voltage biomedical applications [3], since in these applications low power is a key requirement and some non-linearity can be tolerated. There are ISM bands at 450 MHz and 900 MHz and a WMTS band at 600 MHz, for which the circuit proposed here can be a good alternative to the conventional solutions.

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

In recent years, wireless communications applications have been developed due to the huge demand for mobile equipments. Associated with the mobility, the equipment small size and low cost are important requirements. LNAs are used in all wireless receivers. In this thesis, low area CMOS inductorless RC LNAs with low power and low noise are investigated.

In chapter 4 is presented the design of a low power LNA with noise and distortion cancellation based on the combination of a common-gate (CG) and a common-source (CS) stages, using active loads. The replacement of resistor loads by transistors reduces the area and cost and adds a new degree of freedom in the design, which can be used to maximize the LNA gain and minimize the noise figure. Moreover, by proper biasing of the CS stage, the impact on circuit linearity can be minimized. This improvement is due to the higher dynamic output resistance of the active loads for the same DC voltage drop. Moreover, the use of active loads allows the control of the LNA gain and the reduction of the supply voltage. Switches are avoided, and the input impedance and the noise figure are not affected.

In chapter 5, two techniques are proposed to boost the LNA gain without degrading the input matching constraint. These two techniques are called double feedforward (DFF) and double feedback (DFB), and both use local feedback. Moreover, the possibility of reducing the supply voltage from 1.2 V to 0.6 V is investigated. Two circuit prototypes in a 130 nm standard CMOS technology at 1.2 V and 0.6 V have been designed and simulated to demonstrate the proposed techniques. Comparing the two approaches, it is found that DFB leads to the highest gain and the lowest NF, leading to the highest FOM. The disadvantages are the increase of the circuit non-linearity and the reduction of the bandwidth.

In chapter 6 measurement results of an LNA implemented in a 130 nm CMOS technology have been presented. For comparison, the performance of a conventional LNA with resistor loads is also shown . For a fair comparison, both circuits have the same power consumption of 4.8 mW, and the same test circuitry. For the LNA with active loads, a gain improvement of about 3 dB and a NF reduction of about 0.5 dB is obtained, with an IIP3 higher than 0 dBm. These results shows that the use of active loads is a viable alternative when compared with the state-of-the art.

Two receiver front-end circuit prototypes are presented in a 130 nm CMOS technology using 1.2 V supply. These demonstrators are especially useful for low power and low voltage operation in biomedical applications (ISM and WMTS bands), but they have a wider range of application. Simulation and measurement results are presented for the receiver using the DFB LNA (presented in chapter 5) and are compared with the results for a receiver using the LNA using active loads (presented in chapter 4), but without gain boosting. In the band of interest (100 MHz to 1.4 GHz), the DFB LNA leads to gain improvement of more than 3 dB and the NF is reduced by 2 dB for a power consumption of 5.4 mW, when compared with an LNA with active loads without feedback.

7.2 Future Work

The following research topics are suggested:

- The measurement setup for the DFB LNA should be improved, by measuring it in a separate single chip circuit. This would allow to directly measure the LNA parameters more accurately and avoiding extrapolation.
- The possibility of using the active loads in saturation, and designing the receiver in current-mode. This, will require a DC regulation loop, since the DC biasing is sensitive to mismatches. Moreover, a detailed study about noise and linearity is required.
- The influence of the current-source on the NF of the complete LNA, by using feedback topologies avoiding a constant voltage biasing.
- The possibility of using active inductors in the LNA loads, in order to increase the gain and extend the bandwidth.
- A complete study of the discrete-time mixer with parametric amplification. By using parametric amplification, a traditional "passive" mixer with a voltage gain higher than 1 can be designed, thus, minimizing the NF of the complete receiver. This work has already started, and has led to some publications [59].
- A complete study of the proposed LNA topologies in deep submicron CMOS technologies (65 nm and 28 nm). This can lead to a better performance in terms of bandwidth, that is the main limitation of the proposed LNA with active loads and gain boosting.

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